NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE30H32VD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

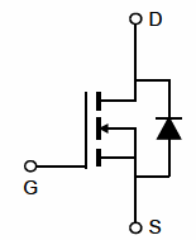
- V_{DS} =30V ,I_D =320A
  $R_{DS(ON)}$ < 1.6mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ < 2.4mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

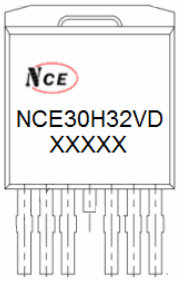
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

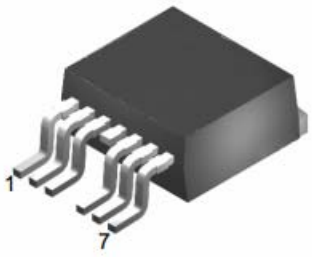
100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-263-7L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30H32VD	NCE30H32VD	TO-263-7L	-	-	-

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous (Silicon Limited)	I_D	320	A
Drain Current-Continuous(T_C=100℃) (Silicon Limited)	I_D (100℃)	226	A
Pulsed Drain Current	I_{DM}	1280	A
Maximum Power Dissipation	P_D	320	W
Derating factor		2.13	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	1600	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.47	℃/W

Electrical Characteristics (T_A=25℃unless otherwise noted)

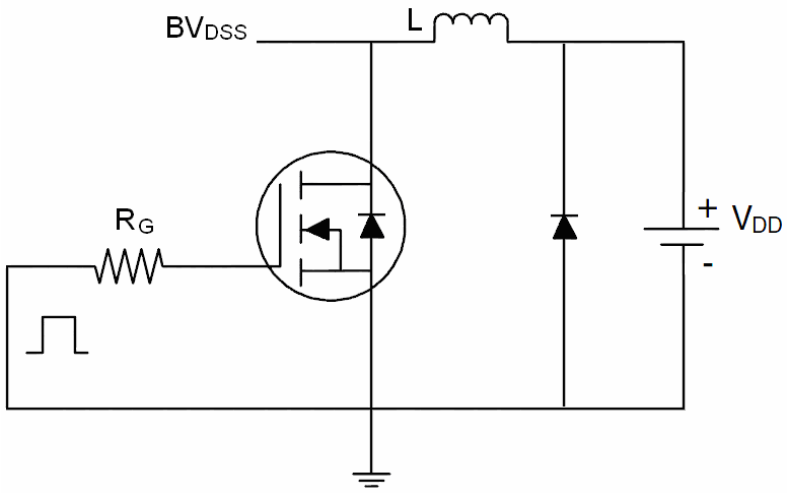
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=160A	-	1.2	1.6	mΩ
		V_{GS}=4.5V, I_D=160A	-	1.6	2.4	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=160A	50	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	13873	-	PF
Output Capacitance	C_{oss}		-	1672	-	PF
Reverse Transfer Capacitance	C_{rss}		-	1508	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,R_L=15Ω, R_G=2.5Ω,V_{GS}=10V	-	18	-	nS
Turn-on Rise Time	t_r		-	200	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	85	-	nS
Turn-Off Fall Time	t_f		-	125	-	nS
Total Gate Charge	Q_g	I_D=160A,V_{DD}=15V,V_{GS}=10V	-	231	-	nC
Gate-Source Charge	Q_{gs}		-	27.5	-	nC
Gate-Drain Charge	Q_{gd}		-	55	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=160A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	320	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, I_F = 160A di/dt = 100A/μs (Note3)	-	70		nS
Reverse Recovery Charge	Qrr		-	180		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

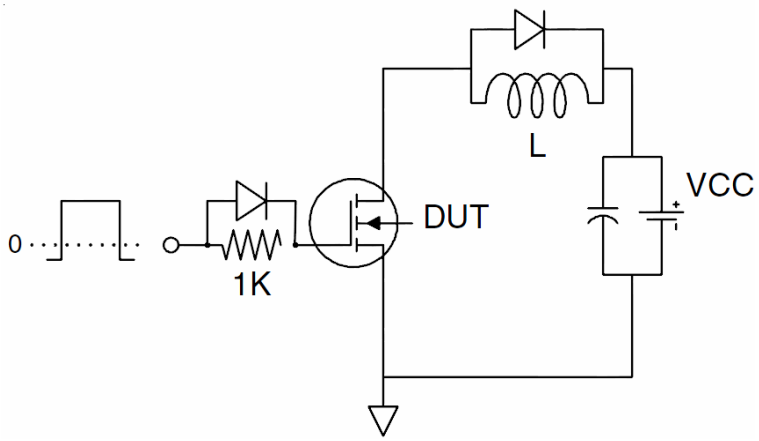
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω

Test circuit

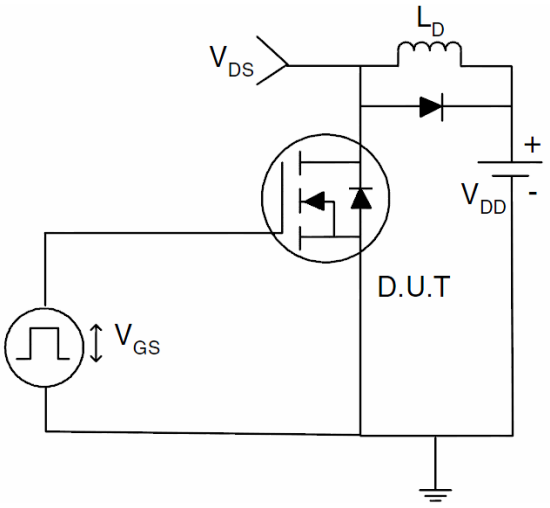
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit：



Typical Electrical and Thermal Characteristics (Curves)

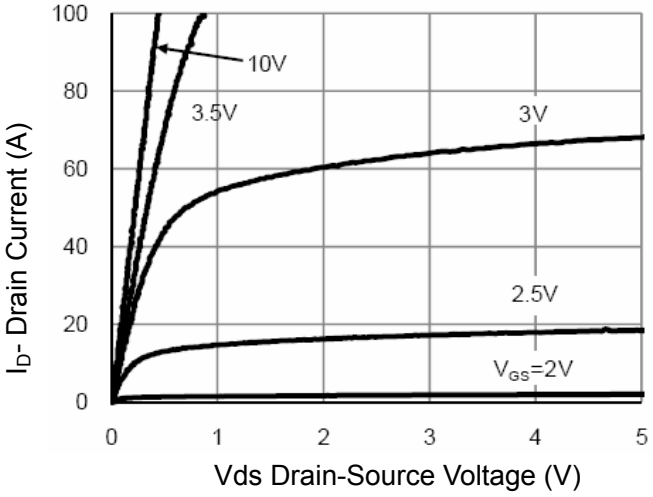


Figure 1 Output Characteristics

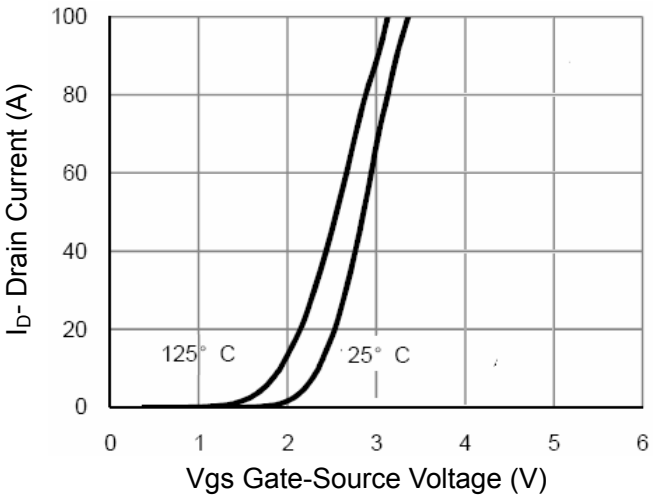


Figure 2 Transfer Characteristics

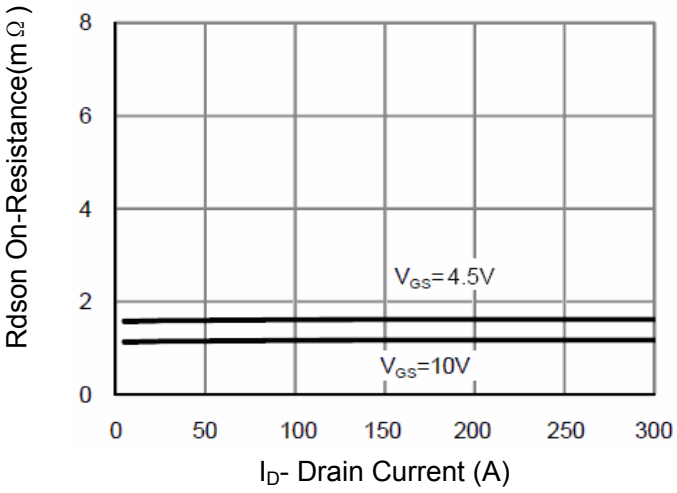


Figure 3 Rdson- Drain Current

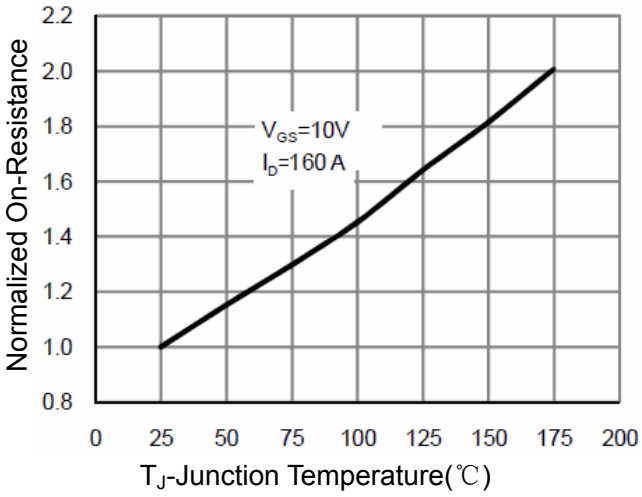


Figure 4 Rdson-JunctionTemperature

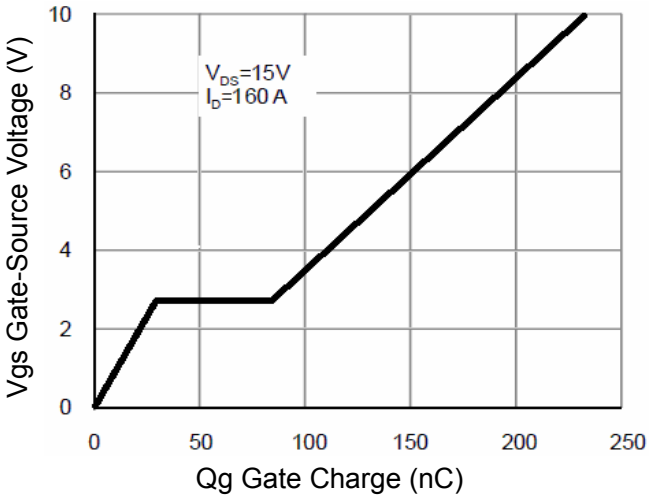


Figure 5 Gate Charge

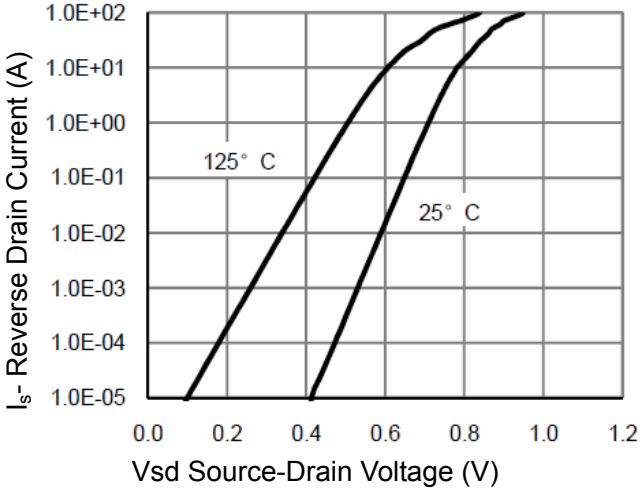


Figure 6 Source- Drain Diode Forward

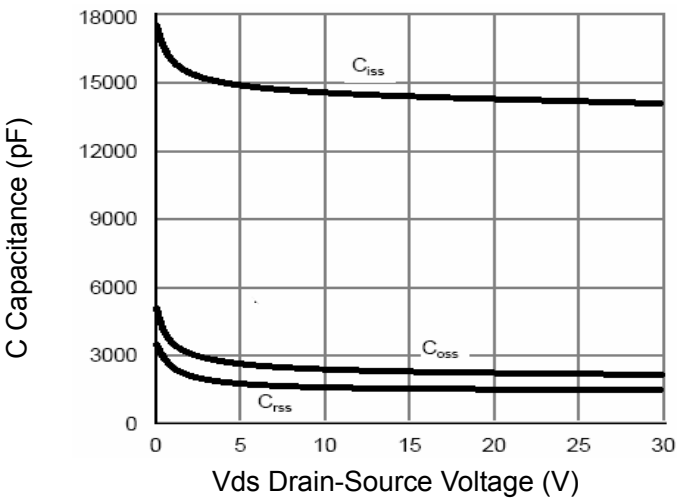


Figure 7 Capacitance vs Vds

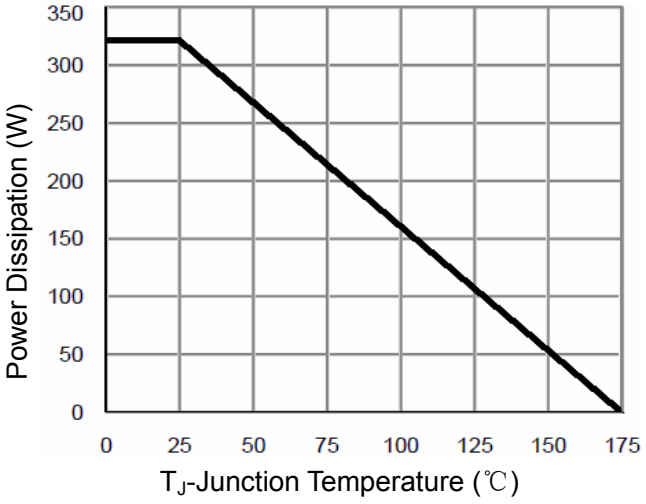


Figure 9 Power De-rating

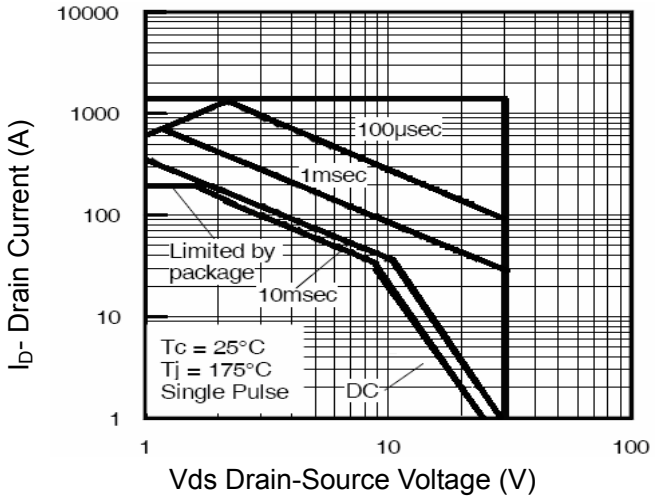


Figure 8 Safe Operation Area

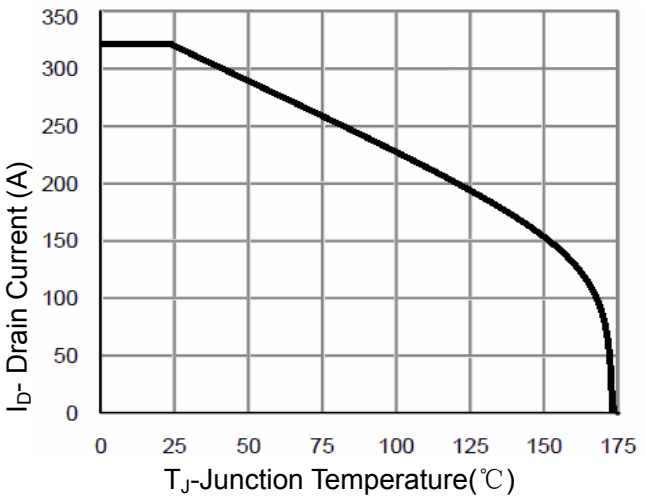


Figure 10 Current vs Junction Temperature

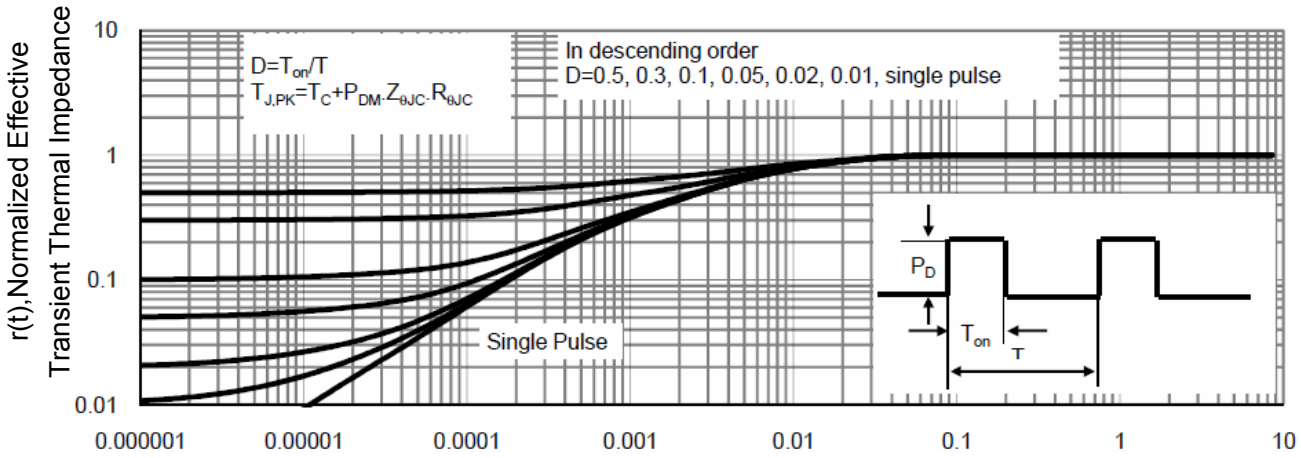
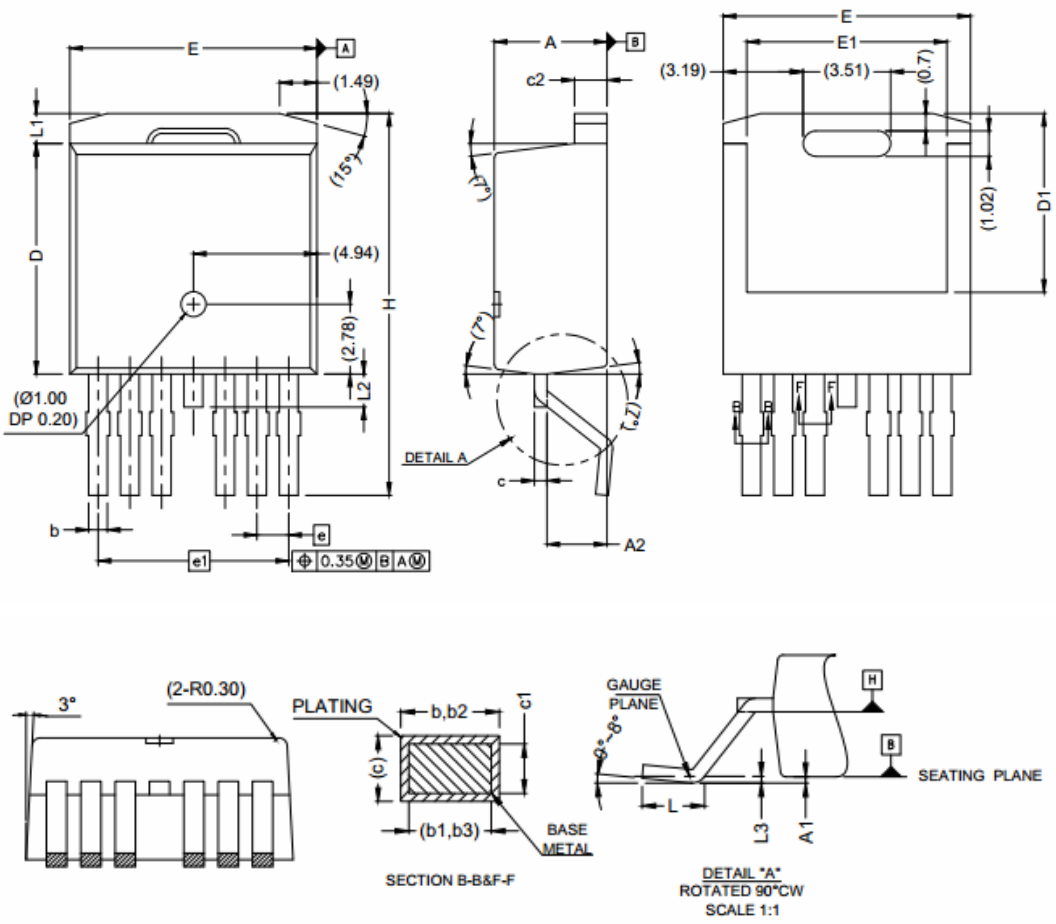


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-7L Package Information



SYMBOL	MIN	MAX
A	4.30	4.70
A1	-	0.254
A2	2.20	2.60
b	0.65	0.85
b1	0.65	0.80
b2	0.80	1.00
b3	0.80	0.95
c	0.45	0.60
c1	0.45	0.55
c2	1.25	1.40
D	9.00	9.40
D1	6.86	7.42
E	9.68	10.08
E1	7.70	8.30
e	1.27 BSC	
e1	7.62 BSC	
L	1.78	2.79
L1	-	1.60
L2	-	1.78
L3	0.25BSC	
H	14.61	15.88

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