CL185X
QR-PWM反激式控制器(SSR)

概述 General Description

◆ CL185X is a higher integrated PWM flyback power switch, which integrated various HV-MOSFET. It provides several functions to enhance the efficiency to meets the criteria of global standards such as DoE Level VI and EU CoC V5 Tier-2. Meantime, it also provides excellent EMI-improved solution, and also built in complete protection.

◆ CL185X is a multi-mode controller. At full load, the IC operates in fixed frequency CCM mode or QR mode based on the AC line. In this way, high efficiency in the universal input voltage at full load can achieved. At normal load, It operates in QR mode. When the load goes low, it operates in Green mode with Valley switching for high efficiency. When the load is very small, the IC operates in Burst mode to minimize the standby power loss. As a result, high efficiency can be achieved in the whole loading range.

◆CL185X also built-in the leading-edge blanking (LEB) of the current sensing and feedback loop to screen the spike noise form any input signal. The internal slope compensation can limit the constant output over universal AC input range. The sawtooth over frequency function for EMI improved solution.

◆ Meanwhile, CL185X also provides various protection, such as, OLP (Over Load Protection) ,VDD OVP (Over Voltage Protection) , Output OVP and VDD OVP to prevent the circuit damage from the abnormal conditions.

◆CL185X is available in SOP7 and DIP7
◆CL185X works with current sensing synchronous rectifier controllers, such as CLR6300, to achieve higher conversion efficiency and very compact power density..

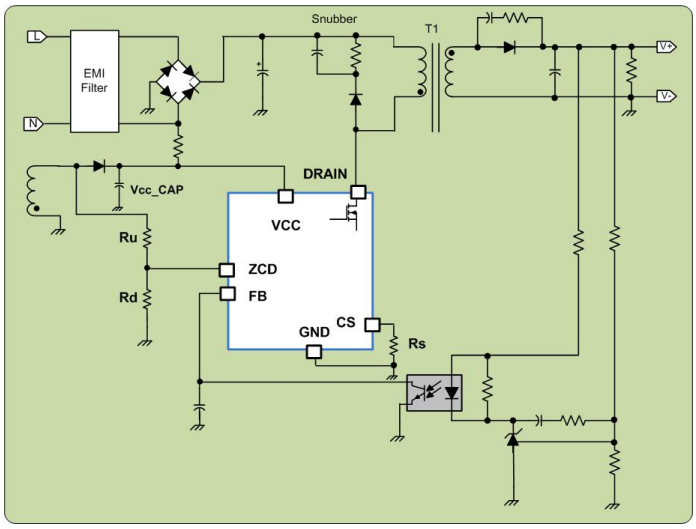
特点 Feature

- 65KHz fix frequency mode at PWM Mode
- Internal 12ms Soft-start in 65KHz
- Very low startup current (<6 uA)
- 0.5mA ultra-low operating current at light load
- Programmable adaptive burst control for light-load efficiency with low output ripple and audible noise suppression.
- Programmable adaptive Frequency Shuffling and Slope Compensation @ QR and PWM Mode
- Current mode control with Cycle-by-Cycle current limit
- Built-in slope and load regulation compensation
- LEB (Leading-edge blanking) on CS Pin
- UVLO (Under voltage lockout)
- Fault Protections : VDD Over Voltage, ZCD OVP(Over Voltage & UVP (Under Voltage), Output Short-Circuit, Over-Current, OLP (Over load protection) and Pin Fault
- Photo coupler short protection & Feedback open protection
- High voltage CMOS process with excellent ESD protection

应用范围 Application

- Switching AC/DC adapter and battery charger
- ATX standby power
- Open frame switching power and CD(R)
- Set-top-boxes(STB) 384Xreplacement

典型应用电路 Application Circuit

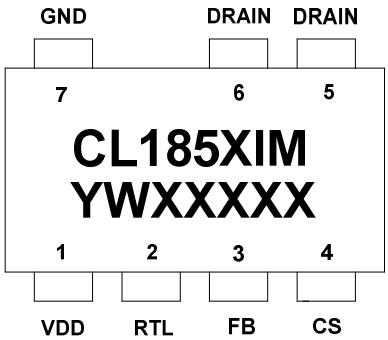


功能和保护选项 Function and Protection Options

Part No.	Package	Freq.	Protection					
		KHZ	VDD OVP	OLP	AUX. OVP	AUX. UVP	CS Open	SDSP
CL185X	**DIP7/SOP7**	65KHz	Hiccup	Hiccup / 65mS	Hiccup	Hiccup	Hiccup	Hiccup

打标说明及管脚分布 Top View/ Marking

DIP7/SOP7

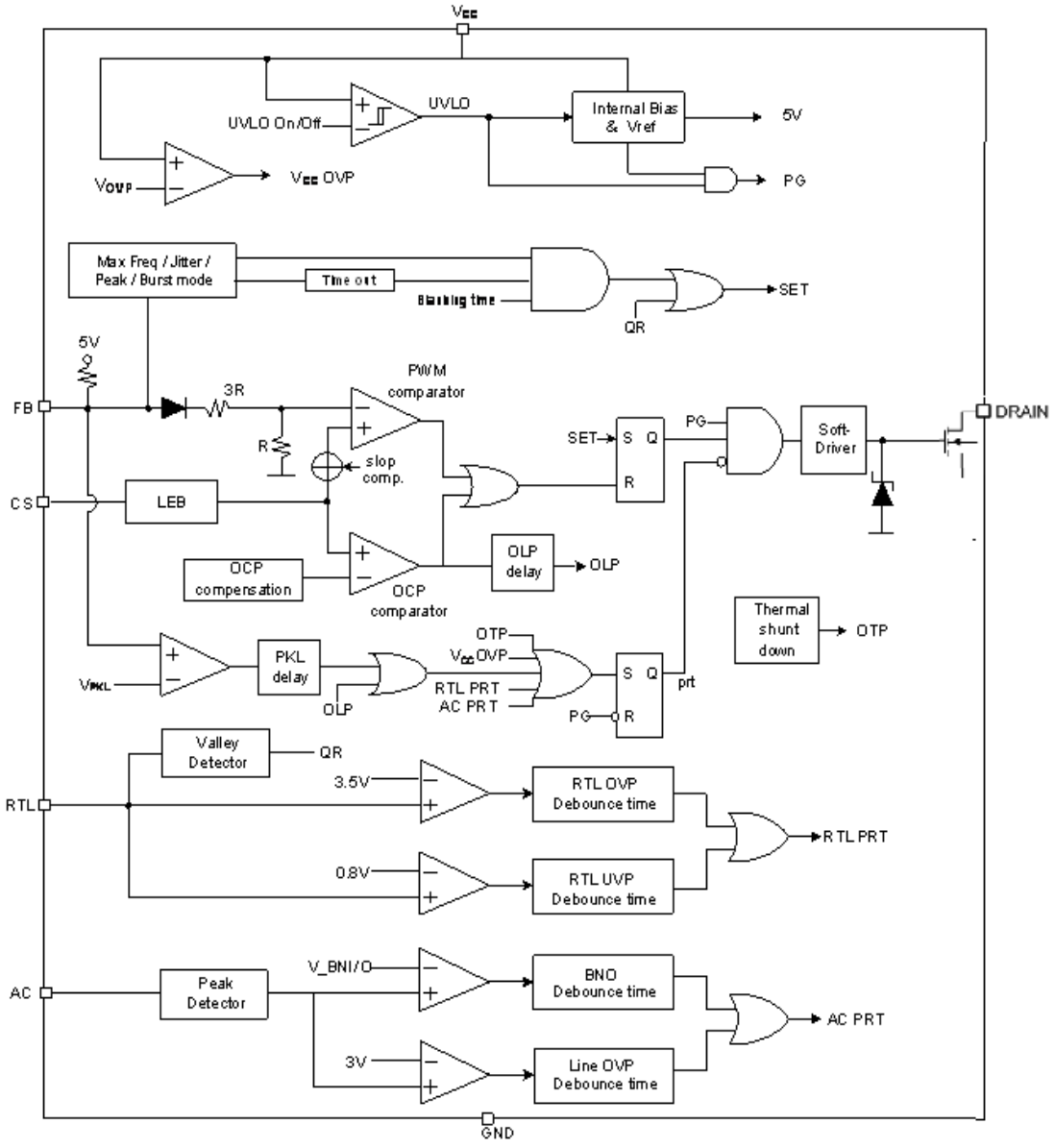


Pin Figure	Silk-screen	Marking Instructions
TheLeft Diagram	CL185X	Chip Type Number
	Y	Year Number
	W	Week Number
	XXXXX	Version Number

管脚功能描述 Pin Assignments and Package Type

SOP7	DIP8	引腳名稱	引腳功能
1	1	VDD	電源供應引腳。
2	2	RTL	可編程多重模式引腳，輔繞線圈電壓偵測、去磁引腳及輸出電壓過壓保護設定。
3	3	FB	電壓回饋引腳。藉由光耦合器連結控制回路達到輸出調節。
4	4	CS	電流感測引腳。電流感測電阻置於此引腳與地之間，用以設定電流限制。
5	5	DRV	柵極驅動輸出引腳。
6/7	6/7	GND	控制器的地端。

结构框图 Block Diagram



最大额定值 Absolute Maximum Ratings

Parameter Symbol		Symbol	Limit Values		Unit	Remark
			Min.	Max		
供應輸入電壓，電源供應引腳(VDD)到地 VDD		V_{DD}	-0.3	32	V	
電壓回饋(FB),電流檢測 CS,多重模式(RTL)引腳到地		V_{FB},V_{CS},V_{RTL}	-0.3	7	V	
柵極引腳(DRV)到地		V_{GATE}	-0.3	V_{DD}+0.3	V	
操作溫度 Operation Junction Temperature		Tj		125	℃	
環境操作溫度範圍 Operation Ambient Temperature		TA	-25	85	℃	
儲存溫度範圍 Storage Temperature		T_{stg}	-55	150	℃	
功率耗散，PD @ TA = 25° C Power Dissipation	Ta = 25℃	PD	-	556	mW	SOP7
封裝熱阻抗 I Junction-to-Ambient Thermal Resistance*		θ_{JA}	-	180*2	℃/W	SOP7
封裝熱阻抗 II Junction-to-Case Thermal Resistance**		θ_{JC}	-	39*3	℃/W	SOP7
功率耗散，PD @ TA = 25° C Power Dissipation	Ta = 25℃	PD	-	1.1	W	DIP7
封裝熱阻抗 I Junction-to-Ambient Thermal Resistance*		θ_{JA}		85*2	℃/W	DIP7
封裝熱阻抗 II Junction-to-Case Thermal Resistance**		θ_{JC}		20*3	℃/W	DIP7
焊接溫度 (焊接，10 sec.) Lead temperature (Soldering, 10 sec)			-	260	℃	
靜電耐受度 ESD Voltage Protection	HBM	$V_{ESD-HBM}$	-	3.0	KV	
	MM	V_{ESD-MM}	-	300	V	

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

推荐工作范围 Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
供應輸入電壓 Supply Voltage VDD	VDD	10	25	V	
啟動電阻值 Startup Resistor Value	R_{star}	1	14	MΩ	
環境溫度範圍 Ambient temperature range	T_{opr}	-40	85	℃	
電壓回饋電容值 Capacitance of FB pin	C_{FB}		2.2	nF	

電气特性 DC Electrical Characteristics (VDD =15V, Ta=25°C)

***Supply Voltage (VDD Pin)*:**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Startup Current	I_{DD-ST}		2	5.5	□A	UVLO ON - 0.1V
Operating Current (with 1nF load on DRV pin)	I_{DD-OP}	0.4	0.6	0.8	mA	V_{FB}=0V
	I_{DD-OP}	1.5	2	2.5	mA	V_{FB}=2.5V CL=1nF
	I_{DD-OLP}	0.2	0.35	0.5	mA	保護電流 Protection Current
UVLO (off)	$V_{UVLO-OFF}$	7.5	8	8.5	V	
UVLO (on)	$V_{UVLO-ON}$	17	18	19	V	
VDD OVP Level	V_{OVP}	26	27	28	V	
OVP Debounce Time	T_{OVP}		4		cycle	Guarantee by Design
VDD Simulation mode(ON)	V_{DD-HD_ON}	9.7	10.2	10.7	V	
VDD Simulation mode(OFF)	V_{DD-HD_OFF}	10.2	10.7	11.2	V	

***Voltage Feedback(FB Pin)*:**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	I_{Zero}	0.1	0.14	0.18	mA	V_{FB}=0V
Open Loop Voltage	V_{FB-OP}	4.8	5	5.2	V	FB pin open
Burst mode start voltage(on)	V_{BUR_ON}	0.9	1	1.1	V	RTL Discharge Voltage 2.7
Burst Mode Hysterics	V_{BUR_HY}	0.05	0.1	0.15	V	
Green Mode Threshold	V_{th_GR}		1.5		V	
Green Mode End Threshold	$V_{th\_GR\_end}$		1.1		V	

Current Sensing (CS Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time & Propagation Delay to Output	T_{LEB} +T_{PD}	300	400	500	ns	
Maximum CS Off Voltage	V_{CSTH}	0.65	0.7	0.75	V	
OCP source current	I_{OCP}	18.5		21.5	%	I_{OCP}/I_{AUX}
Over Load Protection	V_{OLP}	0.45	0.5	0.55	V	T_{ON}
Debounce Time of OLP	T_{OLP}	54	64	74	ms	
Short Circuit Protection Voltage	V_{SCP}		0.85		V	
Debounce Time of V_{SCP}	T_{SCP}		2		cycle	

Multiple functions. Auxiliary voltage sense *(RTL Pin):*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output OVP Trigger Point	V_{TH_OVP}	2.9	3	3.1	V	FB>4V
Output OVP Deglitch Time Constant	$T_{\_OVP\_delay}$		4		Cycle	Guarantee by Design
Output UVP Trigger Point	V_{TH_UVP}	0.7	0.8	0.9	V	FB >4V
Output UVP Deglitch Time Constant	$T_{\_OVP\_delay}$		4		Cycle	Guarantee by Design
Positive Clamped voltage	V_{POS}	6		7	V	
Negative Clamped voltage	V_{NEG}	-0.05		0.05	V	
RTL Leading Blanking time	T_{RTL_LEB}		2		us	Guarantee by Design

Timer Section:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F_{Burst}	20	22.5	25	KHz	
PWM Mode Frequency	F_{PWM}	61	65	69	KHz	
Voltage stability of Frequency	F_{PSRR}	-1		+1	%	VDD = 11V~25V
Frequency Shuffling Range	F_{jitter}	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D_{MAX}	75	80	85	%	
Internal Soft Startup Time	T_{SS}	10		15	ms	

On chip Thermal shut down:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
IOTP Level	V_{IOTP}		150		℃	Guarantee by Design
IOTP exit	V_{OOTP}		120		℃	

MOSFET (Drain Pin) :

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Remark
MOSFET Drain-source Breakdown Voltage	BV_{DSS}	VGS=0V ID=250uA	650			V	
Static drain-source on-resistance	$R65_{(on)}$	VGS=10V ID=1A		3.8		Ω	CL1852IM
		VGS=10V ID=2A		1.9		Ω	CL1853OM
		VGS=10V ID=2A		2.4		Ω	CL1854IM
		VGS=10V ID=2A		1.9		Ω	CL1855IM
		VGS=10V ID=2.5A		1.55		Ω	CL1856IM
		VGS=10V ID=2.5A		1.1		Ω	CL1857IM

Application Note

Operation Overview

The CL185X meets the green power requirement and very is suitable for the application for those networking adaptors, TV open frame and various consumer power, which can provide more power efficiency and lower power loss. It also supports various kind of protection for every abnormal environments.

VDD Start-up and Control

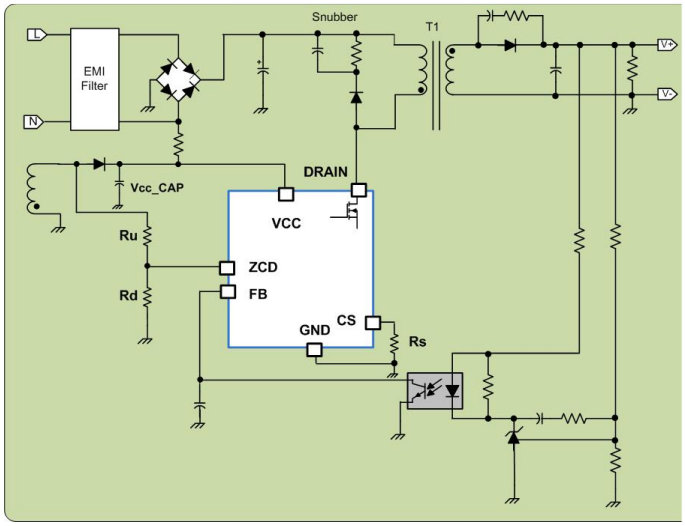


Fig.1

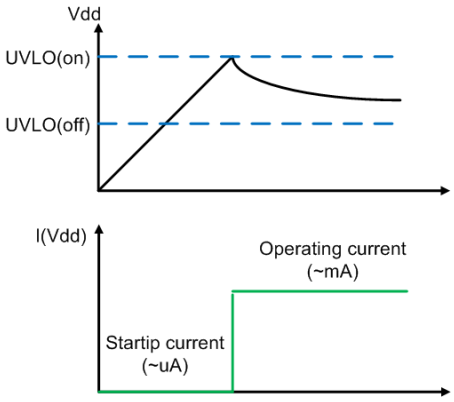


Fig.2

The start-up circuit of CL185X is shown in Fig.1 . Its internal comparator will detect the voltage on the VDD pin, and assures the supply voltage enough to turn on the CL185X. At beginning, the startup current is provided by (R_{st1}/R_{st2}) to charge the capacitor C_{VDD} till VDD get enough voltage (UVLO_ON) to turn on itself, refers to fig.2. Meantime, it goes a step further to deliver the gate drive signal to enable the Aux. winding of transformer , and then provides supply current. The startup current of CL185X is designed to be very low so that C_{VDD} could be charged up above the threshold pf UVLO_on and it starts up quickly.

CL185X series is process with low power mix-mode process (5V and 32V), which max start-up current is below 5.5uA. R-start calculate as below ：

$$\frac{V_{bulk} - V_{UVLO\_ON}}{R_{start}} \square I_{CC-ST}$$

It is trade-off between startup time and a higher startup resistance. Therefore, carefully selects the value of R_{start} and C_{VDD} to optimize the power consumption and startup time.

SS，Soft-start Sequence

CL185X also built-up 12.5ms (typical) soft-start to soften the electrical stress occurring in the power supply during startup, refer to Fig.3. As soon as VDD reaches UVLO_on, the Cs peak voltage is gradually increased from 0.2V to the maximum level, see fig.4.

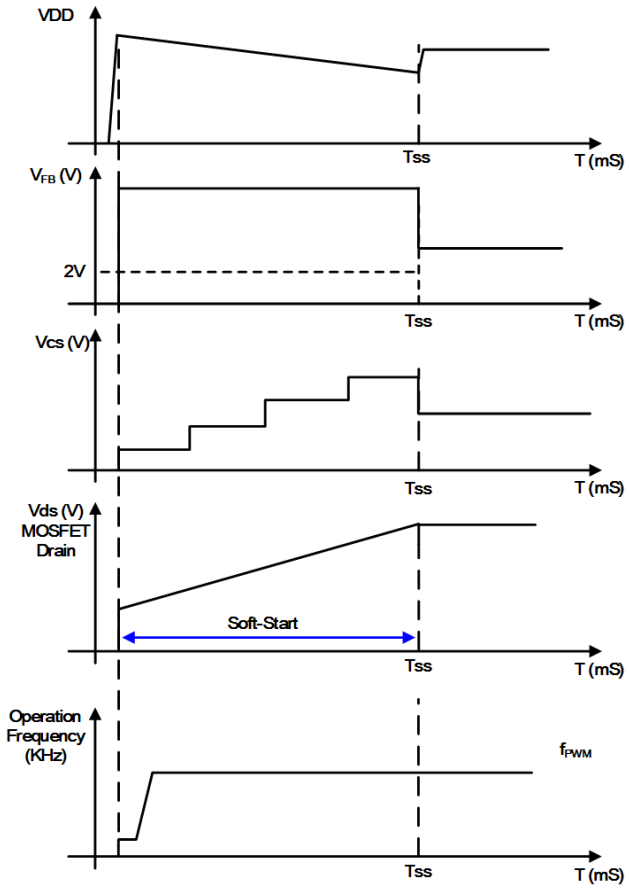


Fig.3

VDD Stimulation Mode

CL185X provides stimulation mode to avoid abnormal re-start-up under the situation of heavy loading to no-load, caused by non-balance of discharge of VDD cap and output cap, which is different with burst mode. The waveform is shown in fig.5.

Condition：V_{FB} < V_{BUR_ON} & V_{DD} <9.5V trigger, Hysterics Voltage 1V

Action：IC fix output F_{Burst} , and V_{CS} keeps as 0.15V

Notice： Design $V_{\_AUX}$ higher than 11V

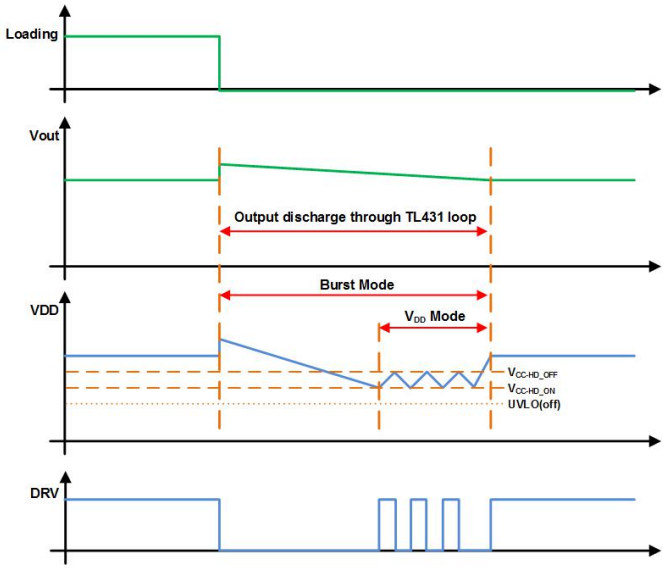


Fig.4

OLP (Over Load Protection)

CL185X has new OLP built-in at CS pin, and its merit of close loop methodology makes audio noise free.

The adjustment of OCP is through RTL and CS, please refer to Fig.5. It detects the status of AC line and output voltage through the resistance divider (Ru,Rd) by the reflection waveform of Aux-winding. At negative cycle, V_{RTL} will keep “0” and output I_{OCP} at CS pin to change the level of slope compensation, please see Fig.5.Therefore, it can modify the Ru and R_{OCP} to get target of OCP @full range. Please follow the procedure as below :

Step 1. Sett R_U=200KΩ , Rd=39KΩ (initial setting) & R_{OCP} = 1KΩ and modifies R_{CS} to target of OCP@90Vac

Step 2. Increase R_{OCP} impedance to reduce OCP and check the OCP of AC full range. Modifies R_{OCP} to make sure the consistency of OCP for AC full range.

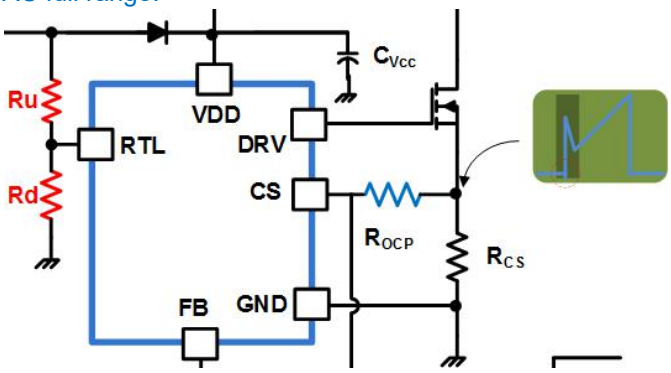


Fig.5

RTL: Demagnetization Detection from RTL pin (QR Mode Detection)

After MOSFET turns off, the current of secondary side diodes goes down to zero , and then the transformer core will be demagnetized completely, see fig.6. At the same time, a quasi resonant signal will be detected from auxiliary winding by RTL pin through the external resister divider.

Programmable V_{O_OVP} & burst mode level

This RTL pin is also used to program the burst level at light load and high output voltage at system open loop . A resistive divider between Aux winding and GND is used to set a voltage at this pin to determine the peak current level when power entries the adaptive burst mode. At the same time, it also detects voltage level of output.

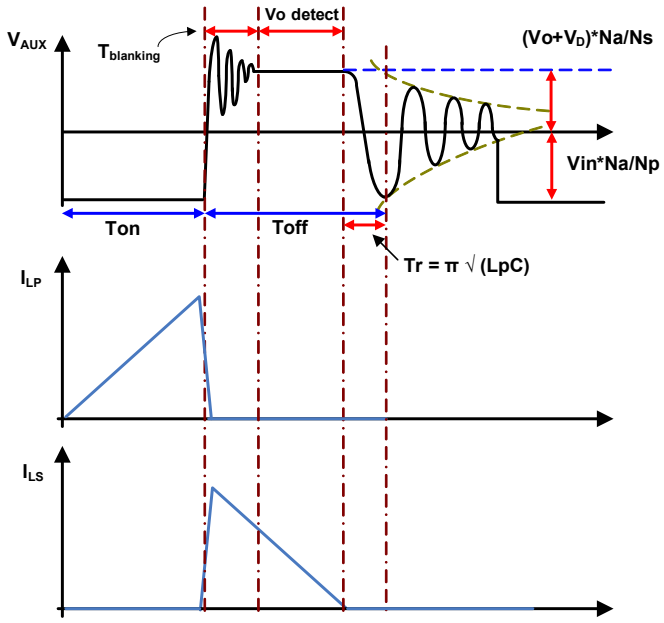


Fig.6

V_{O_OVP}:

- Modifies R_d to target of V_{O_OVP}
- Calculate the ratio of R_d to (R_u+R_d)

$$R_u = 200\text{Kohm};$$

$$\frac{R_d}{R_u + R_d} = \frac{V_{TH\_OVP}}{(V_{O\_OVP} + V_d)} \times \frac{N_s}{N_a}$$

- **Adjust Burst:**

$$V_{BUR\_ON} = (V_O + V_d) \times \frac{N_a}{N_s} \times \frac{R_d}{R_u + R_d} \times 1.7$$

FB，Voltage Feedback Loop

CL185X series adopt current mode control, that is say, the voltage feedback signal is provided from TL431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

(1). R_{bias1} and R_{bias2} to prevent the abnormal output voltage at heavy loading. Generally, we suggest R_{bias1} 100~1KΩ，R_{bias2} 1.5~2.5KΩ

(2). R_{phase}/C_{phase} is for RC phase compensation and prevent oscillate to adjust the value of C_{FB}

(3). Generally, we suggest R_{phase} 1~10KΩ，C_{phase} 0.1uF ， CFB 1~2.2nF

(3). The ratio of R_3 and R_{3A} is depent on the output voltage spec (TL431 ,V= 2.5V)

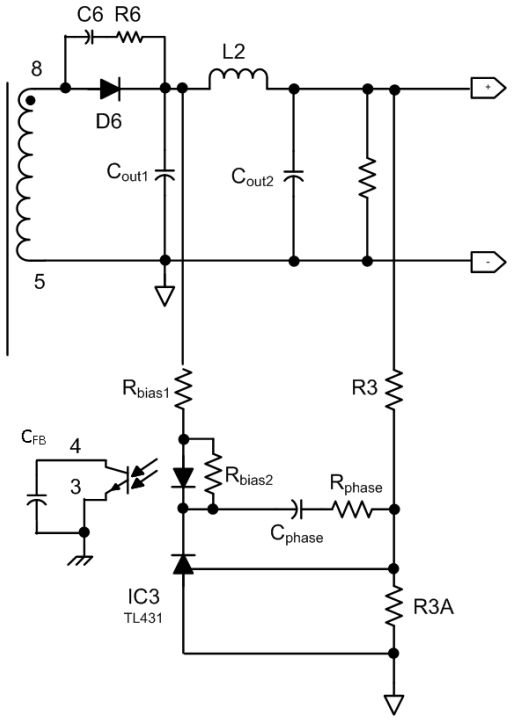


Fig.7

In addition, V_{FB} is also used to determine the green mode level .When V_{FB} is under V_{BUR_ON} , it is under no load or light load condition; at light loading, burst mode can effectively reduces the switching loss. When V_{FB} is larger than V_{BUR_ON}, it will leave away the standby mode. The normal operation of V_{FB} is from V_{BUR_ON} to 2.4V,; meanwhile, short-circuit current is around I_{Zero}.

CS, Current sense Loop

Current mode PWM control mode detects the current command (CS) from the Rsense (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continues conduction mode (CCM) , therefore, CL185X series of built-in high and low slope compensation to avoid the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS

pin being damaged by the unknow negative spike.

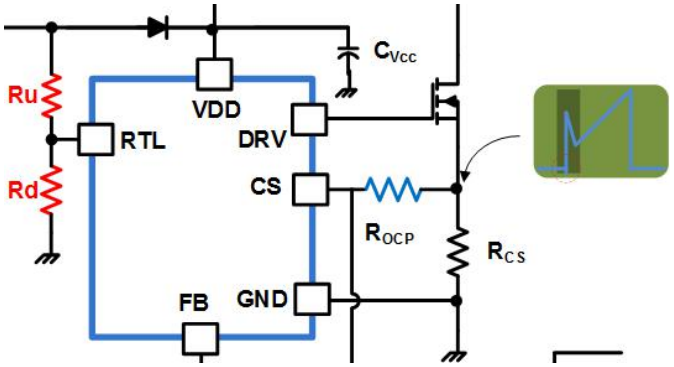


Fig.8

OTP (Over Temperature Protection on CS)

CL185X is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As V_{CS} is greater than 0.5V and continues for 64ms，CS_OTP is triggered, than CL185X is in protection mode till the temperature drops to setting work condition.

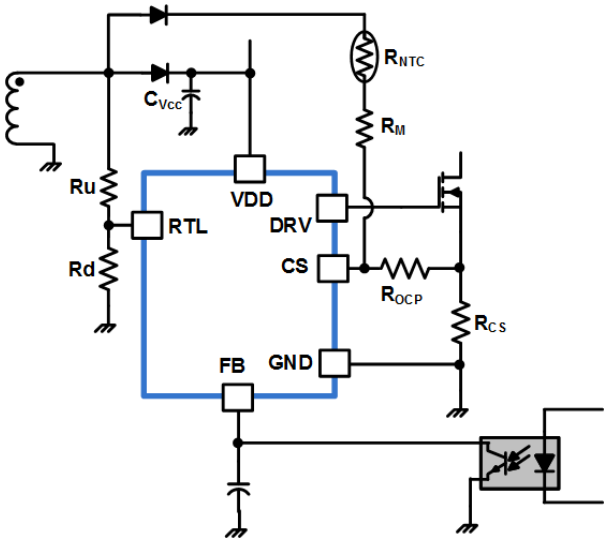


Fig.9

DRV

The driving capability of CL185X is around 450mA, which can support power rate around 60~70W, and it is limited the maximum duty-cycle below 80% to avoid the
transformer saturation.

Typically, the threshold of MOSFET is about 20V, and the maximum clamp voltage of CL185X is 14V to prevent breakdown of MOSFET.

Complete Protection

CL185X integrates various kind of protection to make sure operation safety.

VDD OVP (Over Voltage Protection)

The maximum ratings of the CL185X are around 30V. To prevent the VDD enter breakdown condition, CL185X series are integrated with OVP function on VDD pin. Whenever the VDD voltage is higher than the V_{OVP} threshold, the output gate drive circuit will be turn-off simultaneously and the power MOSFET is turn-off until the next UVLO(on) cycle.

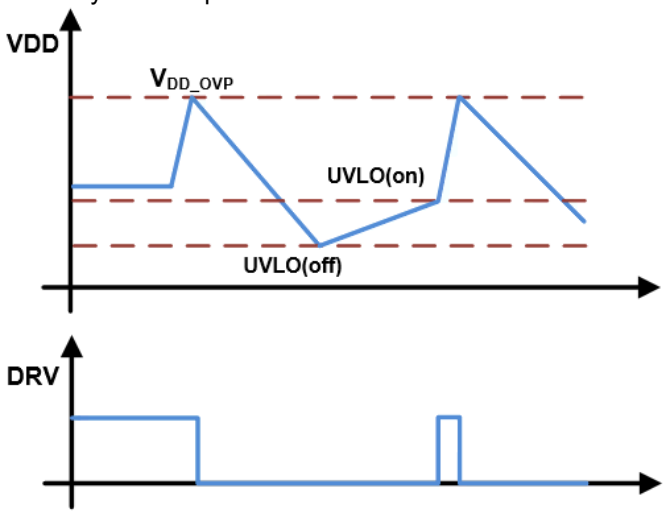


Fig.10

SCP (Short Circuit Protection)

A resistive divider between Aux winding and GND is used to monitor output voltage. When output circuit is short, therefore, as V_{RTL} is lower than 0.8V during date off region, then V_{TH_UVP} is triggered,

CL185X is to enable UVP function in order to reduce input power

SDSP, Secondary Diode Short Protection

After short circuit of 2nd side schottky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high Vds to damage MOSFET.

CL185X detects the inductance current through the resistance, Rcs, of CS pin, and will trigger protection (latch or hiccup) when Vcs higher than 0.85V and sustains 2cycle timing.

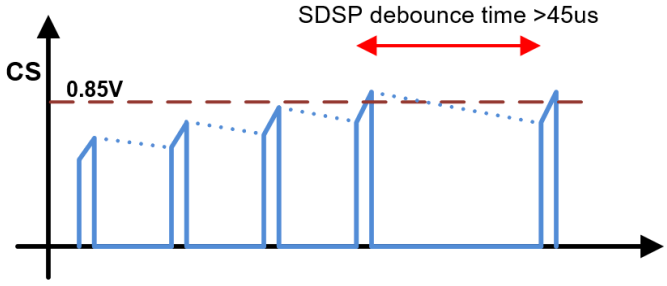


Fig.11

AC, Brown-in/out & Line OVP

CL185X provides real detection of AC line through AC pin connected directly to AC line. When the VDD of CL185X reaches UVLO_ON , it is into the state of AC detection ,and sustains a delay time T_{ADC} .This AC pin is used to program

the AV over and under voltage level through a resistive divider (Ra1/Ra2).

If Vac is lower than below V_{BNI} or higher than V_{LNOVP_HYS}, it will turn-off the output till next cycle to check the condition is removed or not. Even after it turn-off, this pin is continues to detect line status. If Vac is lower than below V_{BNO} or higher than V_{LNOVP} for the timing T_{BNO} and T_{LNOVP}, it will be turn-off , and re-start again. Please refers to fig12.

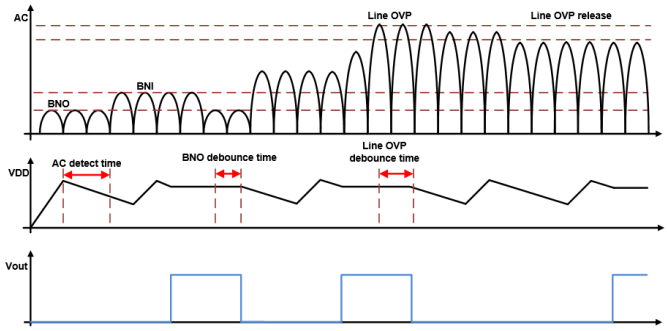


Fig.12

Layout Guide line

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

- **Big current path** : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area
- **Low voltage area :** R devider need to be as near FB_Pin as possible.
- **Secondary Side Schottky :** routing as close as possible
- **Grounding :** (2).(3) and (4) grounding separated with each other, and end connects to (1) ground.
- **RTL :** Ru & Rd as close as possible to avoid noise coupling to trigger OVP.

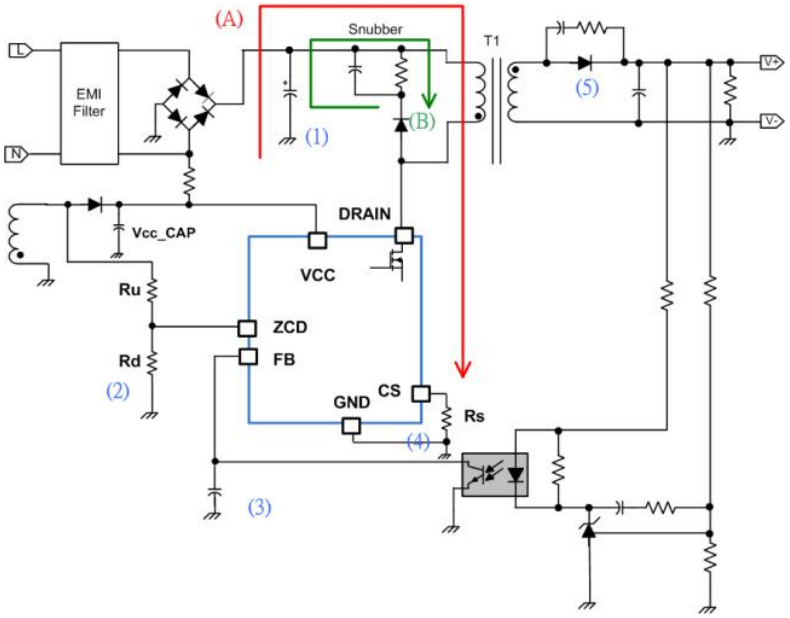
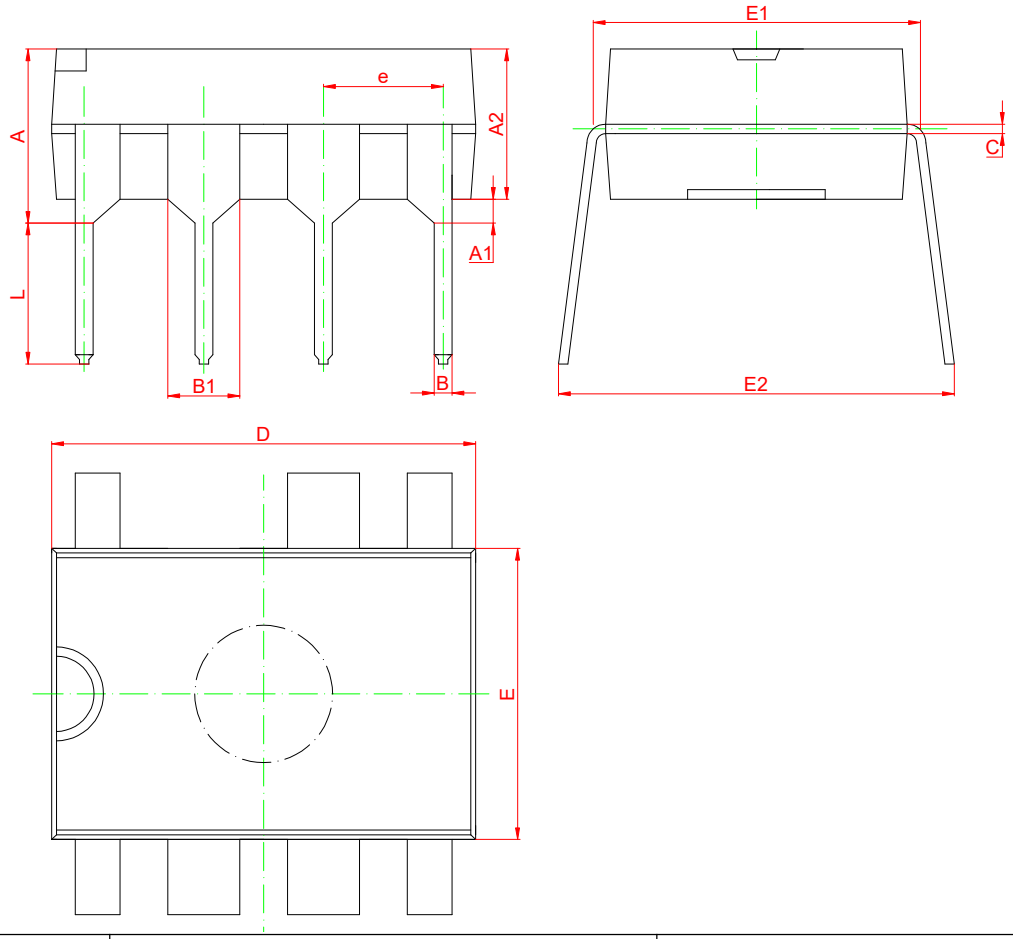


Fig.13

保护功能 **Table 1: Complete Protection**

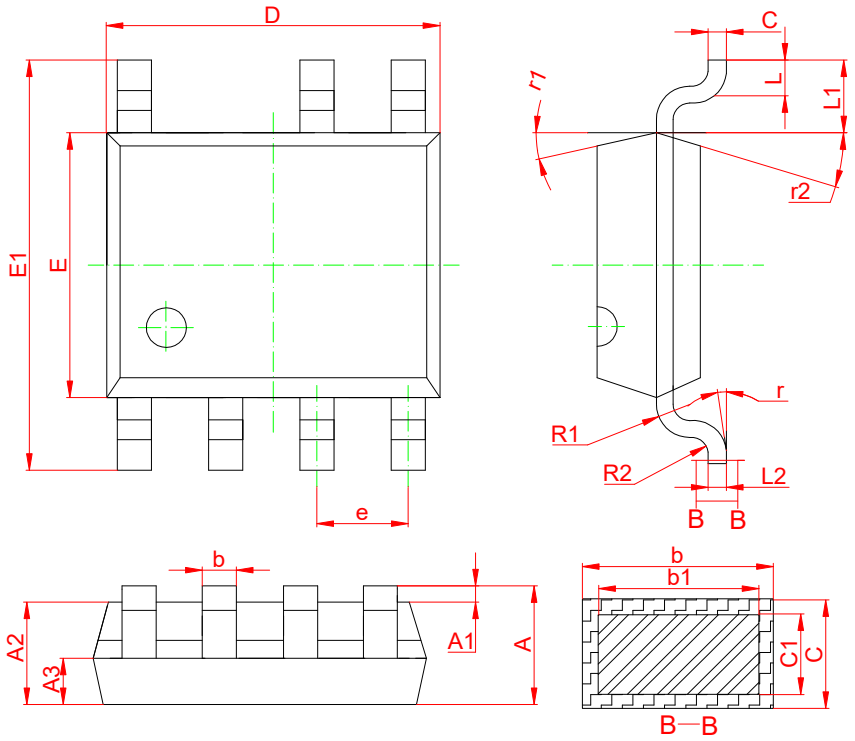
Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VDD OVP	VDD	VDD > 28V
1st	V-Sense	VDD UVLO Off	VDD	VDD < 7.5V
1st	V-Sense	Brown In Fail	AC	V_{AC}<0.85
1st	V-Sense	Brown out	AC	V_{AC}>0.75V
1st	V-Sense	Line OVP	AC	V_{AC}>3.0V
1st	V-Sense	T1 Aux gnd open	RTL	RTL UVP trigger
1st	V-Sense	MOS short/Gate to GND	RTL	RTL UVP trigger
1st	V-Sense	CS pin open	CS	V_{CS}>0.7V after 4 cycles
1st	RTL	RTL upper R open	RTL	RTL UVP：after soft-start RTL<0.85V & FB>4V
1st	RTL	RTL upper R short	RTL	RTL OVP : RTL>3V & FB>4V
1st	RTL	RTL down side open	RTL	RTL OVP : RTL>3V & FB>4V
1st	RTL	RTL down-side short	RTL	RTL UVP：after soft-start time RTL<0.85V & FB>4V
2nd	SDSP	2nd side Schottky short	CS	VCS >0.85V after 4 cycles
2nd	SCP	Output short	RTL	1. 12ms blank time during start-up 2. after 4 cycles 3. RTL UVP = 0.8V & FB>4V trigger
2nd	OVP	Output OVP	RTL	V_{RTL} compares to 3V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS=0.7V
2nd	OLP	OLP	CS	CS > 0.5V
2nd	Short before power on		RTL	1. 12ms blank time at start-up 2. after 4 cycles 3. RTL UVP = 0.8V & FB>4V trigger
2nd	Short after power on		RTL	1. after 4 cycles 2. RTL UVP = 0.8V & FB>4V trigger
IC	Chip OTP			chip OTP at 150 ℃

Package Information：DIP7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540（BSC）		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Package Information：SOP7



Symbol	Min	NOM	Max
A	1.350	1.550	1.750
A1	0.050	0.150	0.250
A2	1.250	1.400	1.650
A3	0.500	0.600	0.700
b	0.380	-	0.510
b1	0.370	0.420	0.470
c	0.170	-	0.250
c1	0.170	0.200	0.230
D	4.800	4.900	5.000
E	3.800	3.900	4.000
E1	5.800	6.000	6.200
e	1.170	1.270	1.370
L	0.450	0.600	0.800
L1	1.040REF		
L2	0.250BSC		
r	0 °	-	8 °
r1	15°	17°	19°
r2	11°	13°	15°

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