

## 概述 General Description

- ◆ CL1850 is a higher integrated PWM flyback power switch, which integrated various HV-MOSFET. It provides several functions to enhance the efficiency to meets the criteria of global standards such as DoE Level VI and EU CoC V5 Tier-2. Meantime, it also provides excellent EMI-improved solution, and also built in complete protection.
- ◆ CL1850 is a multi-mode controller. At full load, the IC operates in fixed frequency CCM mode or QR mode based on the AC line. In this way, high efficiency in the universal input voltage at full load can be achieved. At normal load, It operates in QR mode. When the load goes low, it operates in Green mode with Valley switching for high efficiency. When the load is very small, the IC operates in Burst mode to minimize the standby power loss. As a result, high efficiency can be achieved in the whole loading range.
- ◆ CL1850 also built-in the leading-edge blanking (LEB) of the current sensing and feedback loop to screen the spike noise form any input signal. The internal slope compensation can limit the constant output over universal AC input range. The sawtooth over frequency function for EMI improved solution.
- ◆ Meanwhile, CL1850 also provides various protection, such as, OLP (Over Load Protection) ,VDD OVP (Over Voltage Protection) , Output OVP and VDD OVP to prevent the circuit damage from the abnormal conditions.
- ◆ CL1850 is available in SOT-23-6L and DIP8
- ◆ CL1850 works with current sensing synchronous rectifier controllers, such as CLR66XX, to achieve higher conversion efficiency and very compact power density

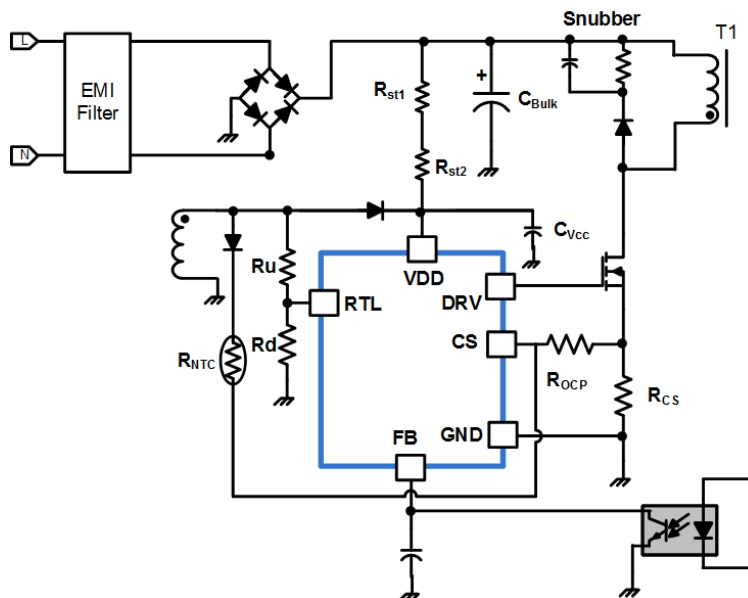
## 应用范围 Application

- ◆ Switching AC/DC adapter and battery charger
- ◆ ATX standby power
- ◆ Open frame switching power and CD(R)
- ◆ Set-top-boxes(STB) 384Xreplacement

## 特点 Feature

- ◆ 65KHz fix frequency mode at PWM Mode
- ◆ Internal 12ms Soft-start in 65KHz
- ◆ Very low startup current (<6 uA)
- ◆ 0.5mA ultra-low operating current at light load
- ◆ Programmable adaptive burst control for light-load efficiency with low output ripple and audible noise suppression.
- ◆ Programmable adaptive Frequency Shuffling and Slope Compensation @ QR and PWM Mode
- ◆ Current mode control with Cycle-by-Cycle current limit
- ◆ Built-in slope and load regulation compensation
- ◆ LEB (Leading-edge blanking) on CS Pin
- ◆ UVLO (Under voltage lockout)
- ◆ Fault Protections : VDD Over Voltage, ZCD OVP(Over Voltage & UVP (Under Voltage), Output Short-Circuit, Over-Current, OLP (Over load protection) and Pin Fault
- ◆ Photo coupler short protection & Feedback open protection
- ◆ High voltage CMOS process with excellent ESD protection

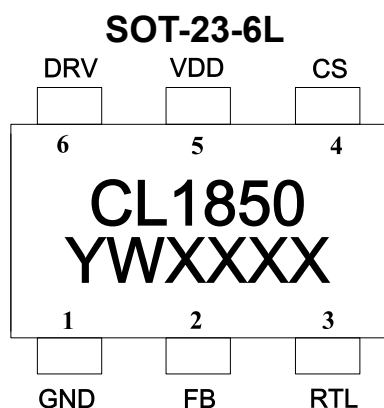
**典型应用电路 Application Circuit**



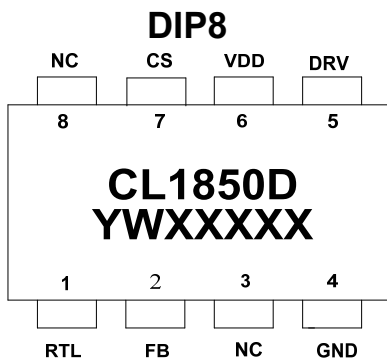
**功能和保护选项 Function and Protection Options**

Part No.	Package	Freq.	Protection					
		KHZ	VDD OVP	OLP	AUX. OVP	AUX. UVP	CS Open	SDSP
CL1850	SOT-23-6L	65KHz	Hiccup	Hiccup / 65mS	Hiccup	Hiccup	Hiccup	Hiccup
CL1850D	DIP8	65KHz	Hiccup	Hiccup / 65mS	Hiccup	Hiccup	Hiccup	Hiccup

**打标说明及管脚分布 Top View/ Marking**



Pin Figure	Silk-screen	Marking Instructions
TheLeft Diagram	CL1850	Chip Type Number
	Y	Year Number
	W	Week Number
	XXXX	Version Number

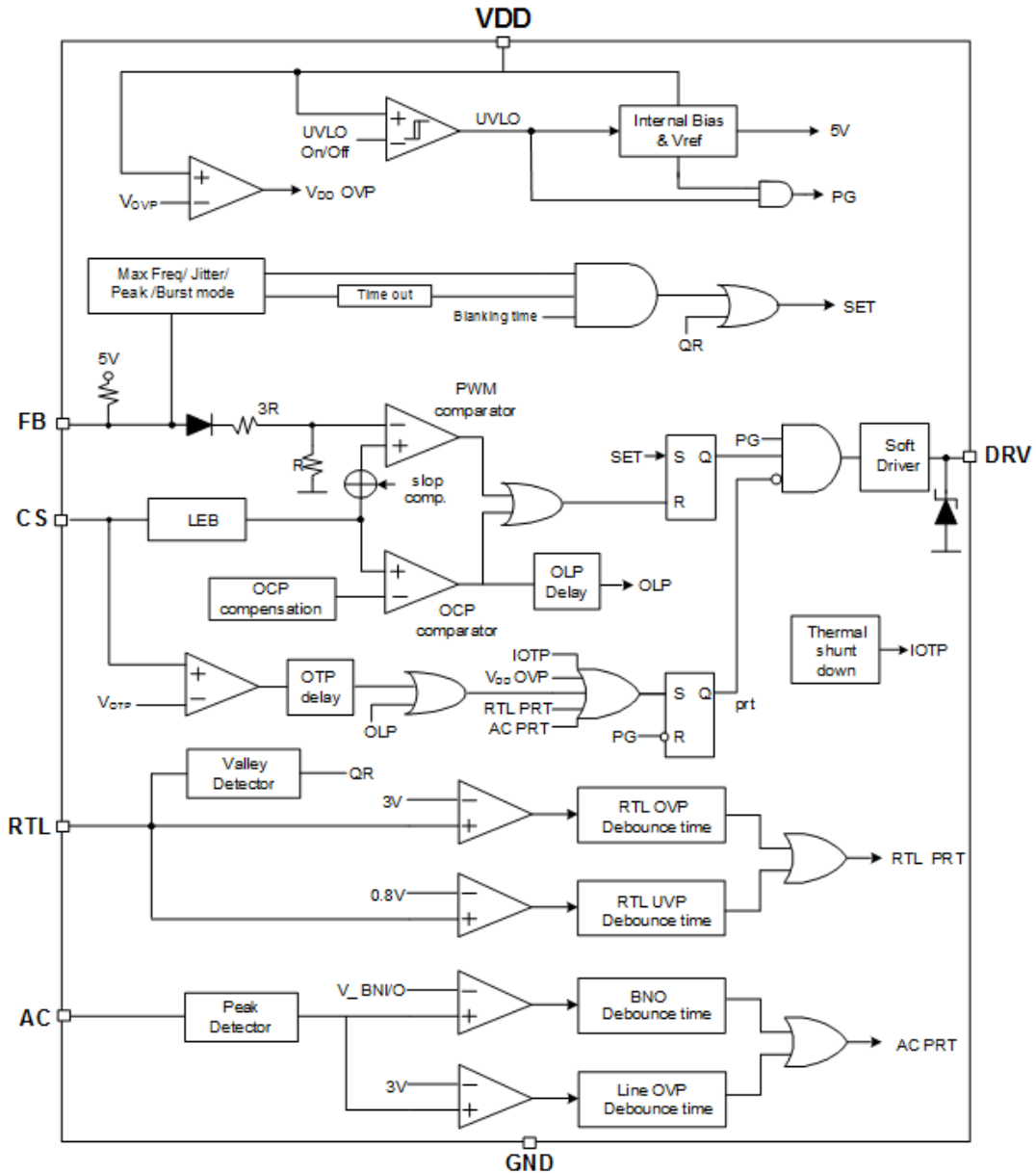


Pin Figure	Silk-screen	Marking Instructions
TheLeft Diagram	CL1850D	Chip Type Number
	Y	Year Number
	W	Week Number
	XXXX	Version Number

### 管脚功能描述 Pin Assignments and Package Type

SOT-23-6L	DIP8	引脚名称	引脚功能
3	1	RTL	可编程多重模式引脚，辅助线圈电压侦测、去磁引脚及输出电压过压保护设定。
2	2	FB	电压回馈引脚。藉由光耦合器连结控制回路达到输出调节。
--	3	NC	悬空。
1	4	GND	控制器的地端。
6	5	DRV	栅极驱动输出引脚。
5	6	VDD	电源供应引脚。
4	7	CS	电流感测引脚。电流感测电阻置於此引脚与地之间，用以设定电流限制。
--	8	NC	悬空。

**结构框图 Block Diagram**



### 最大额定值 Absolute Maximum Ratings

Parameter Symbol	Symbol	Limit Values		Unit	Remark
		Min.	Max		
供應輸入電壓, 電源供應引腳(VDD)到地 VDD	V <sub>DD</sub>	-0.3	32	V	
電壓回饋(FB),電流檢測CS,多重模式(RTL)引腳到地	V <sub>FB</sub> ,V <sub>CS</sub> ,V <sub>RTL</sub>	-0.3	7	V	
柵極引腳(DRV)到地	V <sub>GATE</sub>	-0.3	V <sub>DD</sub> +0.3	V	
操作溫度 Operation Junction Temperature	T <sub>j</sub>	-40	125	°C	
環境操作溫度範圍 Operation Ambient Temperature	T <sub>A</sub>	-25	85	°C	
儲存溫度範圍 Storage Temperature	T <sub>stg</sub>	-55	150	°C	
功率耗散, PD @ TA = 25° C Power Dissipation	PD	-	408	mW	SOT23-6L
封裝熱阻抗 I Junction-to-Ambient Thermal Resistance*	θ <sub>JA</sub>	-	245	°C/W	SOT23-6L
封裝熱阻抗 II Junction-to-Case Thermal Resistance**	θ <sub>JC</sub>	-	55	°C/W	SOT23-6L
封裝熱阻抗 I Junction-to-Ambient Thermal Resistance*	θ <sub>JA</sub>	-	80	°C/W	DIP8
封裝熱阻抗 II Junction-to-Case Thermal Resistance**	θ <sub>JC</sub>	-	20	°C/W	DIP8
焊接溫度 (焊接, 10 sec.) Lead temperature (Soldering, 10 sec)		-	260	°C	
靜電耐受度 ESD Voltage Protection	HBM	V <sub>ESD-HBM</sub>	-	3.0	KV
	MM	V <sub>ESD-MM</sub>	-	300	V

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 推荐工作范围 Recommended Operating Conditions

Parameter Symbol	Symbol	Limit Values		Unit	Remarks
		Min.	Max		
供應輸入電壓 Supply Voltage VDD	VDD	10	25	V	
啟動電阻值 Startup Resistor Value	R <sub>star</sub>	1	14	MΩ	
環境溫度範圍 Ambient temperature range	T <sub>opr</sub>	-40	85	°C	
電壓回饋電容值 Capacitance of FB pin	C <sub>FB</sub>		2.2	nF	

## 电气特性 DC Electrical Characteristics (VDD=15V, Ta=25°C)

### Supply Voltage (VDD Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Startup Current	IDD-ST		2	5.5	□A	UVLO ON - 0.1V
Operating Current (with 1nF load on DRV pin)	IDD-OP	0.4	0.6	0.8	mA	VFB=0V
	IDD-OP	1.5	2	2.5	mA	VFB=2.5V CL=1nF
	IDD-OLP	0.2	0.35	0.5	mA	保護電流Protection Current
UVLO (off)	VUVLO-OFF	7.5	8	8.5	V	
UVLO (on)	VUVLO-ON	17	18	19	V	
VCC OVP Level	VOVP	26	27	28	V	
OVP Debounce Time	TOVP		4		cycle	Guarantee by Design
VCC Simulation mode(ON)	VDD-HD_ON	9.7	10.2	10.7	V	
VCC Simulation mode(OFF)	VDD-HD_OF F	10.2	10.7	11.2	V	

### Voltage Feedback(FB Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Short Circuit Current	IZero	0.1	0.14	0.18	mA	VFB=0V
Open Loop Voltage	VFB-OP	4.8	5	5.2	V	FB pin open
Burst mode start voltage(on)	VBUR_ON	0.9	1	1.1	V	RTL Discharge Voltage 2.7
Burst Mode Hysteresis	VBUR_HY	0.05	0.1	0.15	V	
Green Mode Threshold	Vth_GR		1.5		V	
Green Mode End Threshold	Vth_GR_end		1.1		V	

### Current Sensing (CS Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Leading Edge Blanking Time & Propagation Delay to Output	T <sub>LEB</sub> + T <sub>PD</sub>	300	400	500	ns	
Maximum CS Off Voltage	V <sub>CSTH</sub>	0.65	0.7	0.75	V	
OCP source current	I <sub>OCP</sub>	18.5		21.5	%	I <sub>OCP</sub> /I <sub>AUX</sub>
Over Load Protection	V <sub>OLP</sub>	0.45	0.5	0.55	V	T <sub>ON</sub>
Debounce Time of OLP	T <sub>OLP</sub>	54	64	74	ms	
Over temperature protection	V <sub>OTP</sub>	0.45	0.5	0.55	V	T <sub>OFF</sub>
Debounce Time of OTP	T <sub>OTP</sub>	54	64	74	ms	
OTP Leading Blanking time	T <sub>OTP_LEB</sub>		2		us	Guarantee by Design
Short Circuit Protection Voltage	V <sub>SCP</sub>		0.85		V	
Debounce Time of V <sub>SCP</sub>	T <sub>SCP</sub>		2		cycle	

### Multiple functions. Auxiliary voltage sense (RTL Pin):

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output OVP Trigger Point	V <sub>TH_OVP</sub>	2.9	3	3.1	V	FB>4V
Output OVP Deglitch Time Constant	T <sub>OVP_delay</sub>		4		Cycle	Guarantee by Design
Output UVP Trigger Point	V <sub>TH_UVP</sub>	0.7	0.8	0.9	V	FB >4V
Output UVP Deglitch Time Constant	T <sub>OVP_delay</sub>		4		Cycle	Guarantee by Design
Positive Clamped voltage	V <sub>POS</sub>	6		7	V	

Negative Clamped voltage	V <sub>NEG</sub>	-0.05		0.05	V	
RTL Leading Blanking time	T <sub>RTL_LEB</sub>		2		us	Guarantee by Design

### Driver(DRV Pin) :

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output Low Level	V <sub>OL</sub>			1	V	VDD = 16V, IO=20mA
Output High Level	V <sub>OH</sub>	8			V	VDD = 16V, IO=20mA
Output Clamp Voltage Level	V <sub>G_Clamp</sub>	11	12.5	14	V	VDD = 25V
Rising Time	T <sub>R</sub>	200	300	400	ns	VDD = 16V, CL= 1nF
Falling Time	T <sub>F</sub>	10	30	50	ns	VDD = 16V, CL= 1nF

### Timer Section:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Burst Mode Frequency	F <sub>Burst</sub>	20	22.5	25	KHz	
PWM Mode Frequency	F <sub>PWM</sub>	61	65	69	KHz	
Voltage stability of Frequency	F <sub>PSRR</sub>	-1		+1	%	VDD = 11V~25V
Frequency Shuffling Range	F <sub>jitter</sub>	+/-4	+/-6	+/-8	%	
Maximum duty cycle	D <sub>MAX</sub>	75	80	85	%	
Internal Soft Startup Time	T <sub>SS</sub>	10		15	ms	

### On chip Thermal shut down:

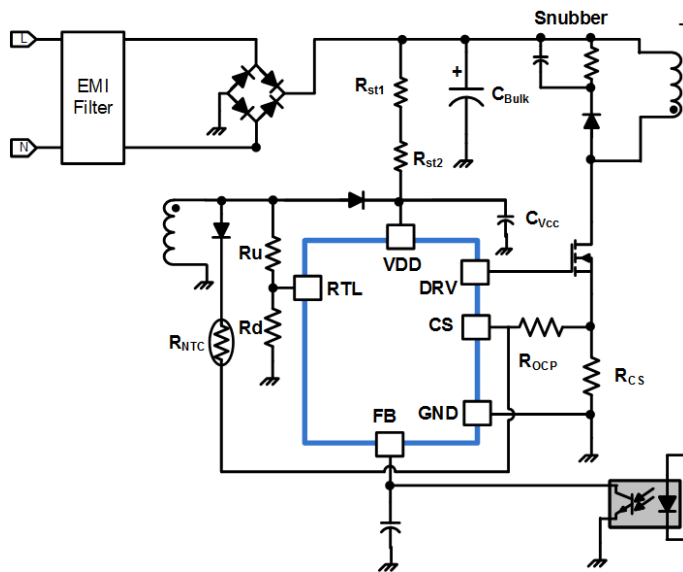
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
IOTP Level	V <sub>IOTP</sub>		150		°C	Guarantee by Design
IOTP exit	V <sub>OOTP</sub>		120		°C	

**应用说明 Application Note**

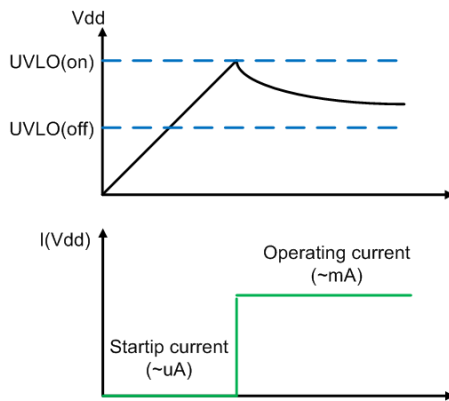
**Operation Overview**

The CL1850 meets the green power requirement and very is suitable for the application for those networking adaptors, TV open frame and various consumer power, which can provide more power efficiency and lower power loss. It also supports various kind of protection for every abnormal environments.

**VDD Start-up and Control**



**Fig.1**



**Fig.2**

The start-up circuit of CL1850 is shown in Fig.1 . Its internal comparator will detect the voltage on the VDD pin, and assures the supply voltage enough to turn on the CL1850. At beginning, the startup current is provided by  $(R_{st1}/R_{st2})$  to charge the capacitor  $C_{VDD}$  till VDD get enough voltage (UVLO\_ON) to turn on itself, refers to fig.2. Meantime, it goes a step further to deliver the gate drive signal to enable the Aux. winding of transformer , and then provides supply current. The startup current of CL1850 is designed to be very low so that  $C_{VDD}$  could be charged up above the threshold pf UVLO\_on and it starts up quickly.

CL1850 series is process with low power mix-mode process (5V and 32V), which max start-up current is below



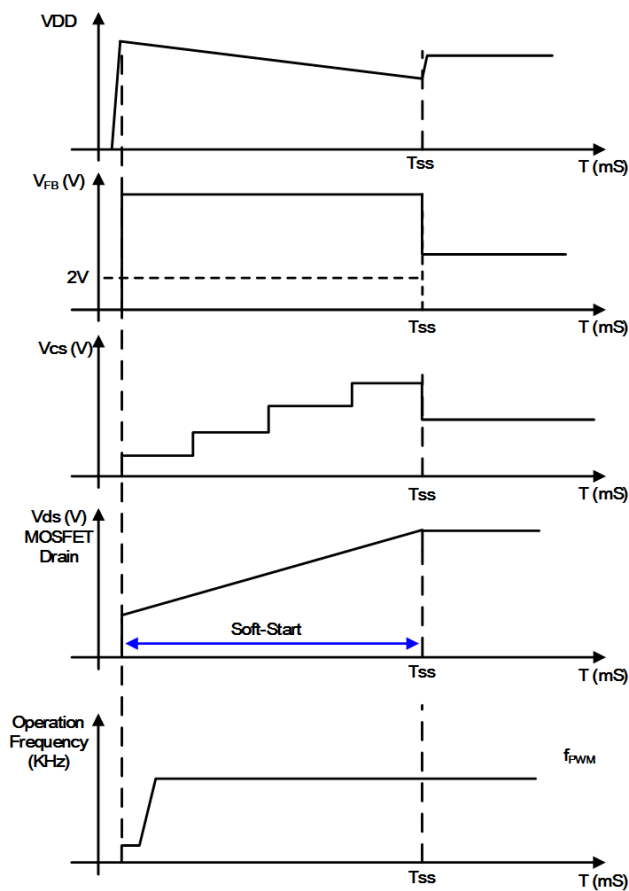
5.5uA. R-start calculate as below :

$$\frac{V_{\text{bulk}} - V_{\text{UVLO\_ON}}}{R_{\text{start}}} \square I_{\text{cc - ST}}$$

It is trade-off between startup time and a higher startup resistance. Therefore, carefully selects the value of  $R_{\text{start}}$  and  $C_{\text{VDD}}$  to optimize the power consumption and startup time.

**SS, Soft-start Sequence**

CL1850 also built-up 12.5ms (typical) soft-start to soften the electrical stress occurring in the power supply during startup, refer to Fig.3. As soon as VDD reaches UVLO\_on, the Cs peak voltage is gradually increased from 0.2V to the maximum level, see fig.4.



**Fig.3**

**VDD Stimulation Mode**

CL1850 provides stimulation mode to avoid abnormal re-start-up under the situation of heavy loading to no-load, caused by non-balance of discharge of VDD cap and output cap, which is different with burst mode. The waveform is shown in fig.5.

Condition:  $V_{\text{FB}} < V_{\text{BUR\_ON}}$  &  $V_{\text{DD}} < 9.5\text{V}$  trigger, Hysteric Voltage 1V

Action: IC fix output F<sub>Burst</sub>, and V<sub>CS</sub> keeps as 0.15V

Notice: Design V<sub>AUX</sub> higher than 11V

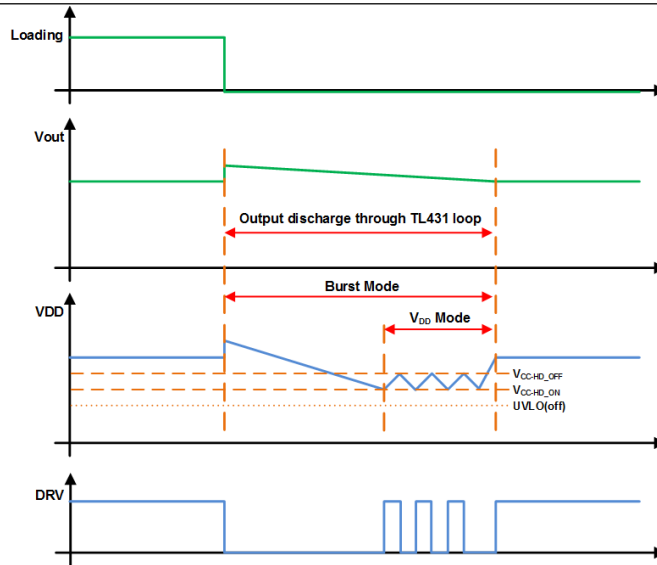


Fig.4

**OLP (Over Load Protection)**

CL1850 has new OLP built-in at CS pin, and its merit of close loop methodology makes audio noise free.

The adjustment of OCP is through RTL and CS, please refer to Fig.5. It detects the status of AC line and output voltage through the resistance divider ( $R_u, R_d$ ) by the reflection waveform of Aux-winding. At negative cycle,  $V_{RTL}$  will keep "0" and output  $I_{OCP}$  at CS pin to change the level of slope compensation, please see Fig.5. Therefore, it can modify the  $R_u$  and  $R_{OCP}$  to get target of OCP @full range. Please follow the procedure as below :

Step 1. Set  $R_u=200K\Omega$  ,  $R_d=39K\Omega$  (initial setting) &  $R_{OCP} = 1K\Omega$  and modifies  $R_{CS}$  to target of OCP@90Vac

Step 2. Increase  $R_{OCP}$  impedance to reduce OCP and check the OCP of AC full range. Modifies  $R_{OCP}$  to make sure the consistency of OCP for AC full range.

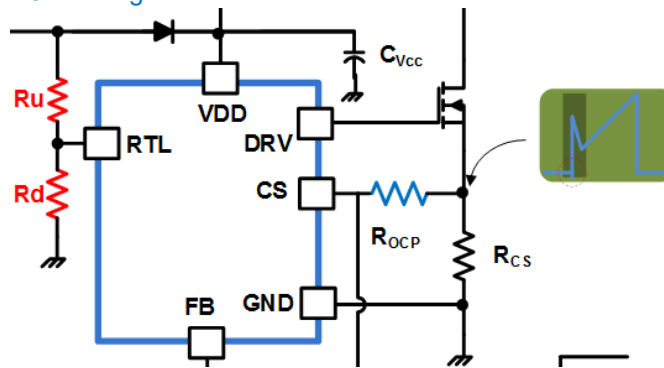


Fig.5

**RTL: Demagnetization Detection from RTL pin (QR Mode Detection)**

After MOSFET turns off, the current of secondary side diodes goes down to zero , and then the transformer core will be demagnetized completely, see fig.6. At the same time, a quasi resonant signal will be detected from auxiliary winding by RTL pin through the external resistor divider.

**Programmable  $V_{O\_ovp}$  & burst mode level**

This RTL pin is also used to program the burst level at light load and high output voltage at system open loop . A resistive divider between Aux winding and GND is used to set a voltage at this pin to determine the peak current level when power

enters the adaptive burst mode. At the same time, it also detects voltage level of output.

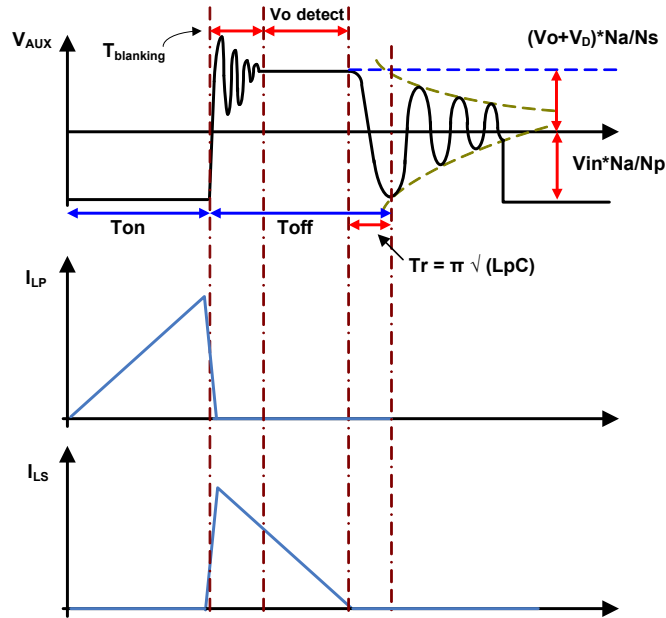


Fig.6

**V<sub>O\_OVP</sub>:**

- Modifies R<sub>d</sub> to target of V<sub>O\_OVP</sub>
- Calculate the ratio of R<sub>d</sub> to (R<sub>u</sub>+R<sub>d</sub>)

R<sub>u</sub> □ 200Kohm;

$$\frac{R_d}{R_u + R_d} \approx \frac{V_{TH\_OVP}}{(V_{O\_OVP} - V_d)} \approx \frac{N_s}{N_a}$$

**□ Adjust Burst:**

$$V_{BUR\_ON} \approx (V_o - V_d) \approx \frac{N_a}{N_s} \approx \frac{R_d}{R_u + R_d} \approx 1.7$$

**FB, Voltage Feedback Loop**

CL1850 series adopt current mode control, that is say, the voltage feedback signal is provided from TL431 at secondary side through the photo-coupler to FB pin and compare to the current signal sensing from Cs pin at primary side of MOS current to control the on/off of MOSFET.

In order to enhance light load efficiency, the loss of the feedback resistor in parallel with photo-coupler is reduced. Due to small feedback resistor current, shunt regulator selection and minimum regulation current design have to considered more carefully to make sure it's able to regulate under low cathode current.

To make sure the stability of feedback is very important. Unstable feedback signal will introduce output oscillate or audio noise. You can monitor the ripple & Noise of output to adjust the phase and gain margin of close loop.

(1). R<sub>bias1</sub> and R<sub>bias2</sub> to prevent the abnormal output voltage at heavy loading. Generally, we suggest R<sub>bias1</sub> 100~1KΩ, R<sub>bias2</sub> 1.5~2.5KΩ

(2). R<sub>phase</sub>/C<sub>phase</sub> is for RC phase compensation and prevent oscillate to adjust the value of C<sub>FB</sub>

- (3). Generally, we suggest  $R_{\text{phase}} = 1 \sim 10\text{K}\Omega$ ,  $C_{\text{phase}} = 0.1\mu\text{F}$ ,  $C_{\text{FB}} = 1 \sim 2.2\text{nF}$
- (3). The ratio of  $R_3$  and  $R_{3A}$  is dependent on the output voltage spec (TL431,  $V = 2.5\text{V}$ )

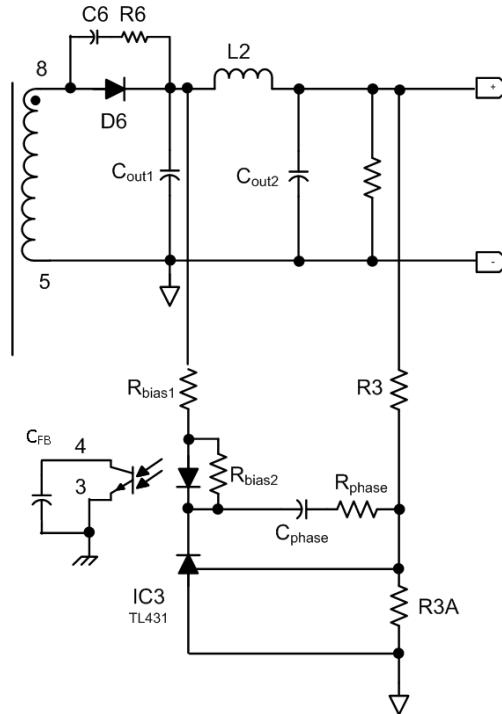


Fig.7

In addition,  $V_{\text{FB}}$  is also used to determine the green mode level. When  $V_{\text{FB}}$  is under  $V_{\text{BUR\_ON}}$ , it is under no load or light load condition; at light loading, burst mode can effectively reduce the switching loss. When  $V_{\text{FB}}$  is larger than  $V_{\text{BUR\_ON}}$ , it will leave away the standby mode. The normal operation of  $V_{\text{FB}}$  is from  $V_{\text{BUR\_ON}}$  to  $2.4\text{V}$ ; meanwhile, short-circuit current is around  $I_{\text{zero}}$ .

### CS, Current sense Loop

Current mode PWM control mode detects the current command (CS) from the  $R_{\text{sense}}$  (the primary MOSFET current sense resistor) and voltage command from photocoupler (FB) to determine whether the system reaches a stable or not. There is a potential risk of sub-harmonic when the duty of flyback methodology is larger than 50% and the operation under continuous conduction mode (CCM), therefore, CL1850 series of built-in high and low slope compensation to avoid the sub-harmonic risk.

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. Meanwhile, it is strongly recommended to put a suitable R-C filter for higher power application to prevent the CS pin being damaged by the unknown negative spike.

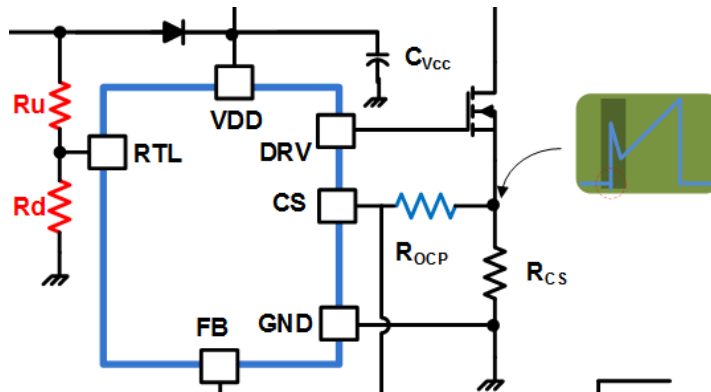


Fig.8

**OTP (Over Temperature Protection on CS)**

CL1850 is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As  $V_{CS}$  is greater than 0.5V and continues for 64ms, CS\_OTP is triggered, then CL1850 is in protection mode till the temperature drops to setting work condition.

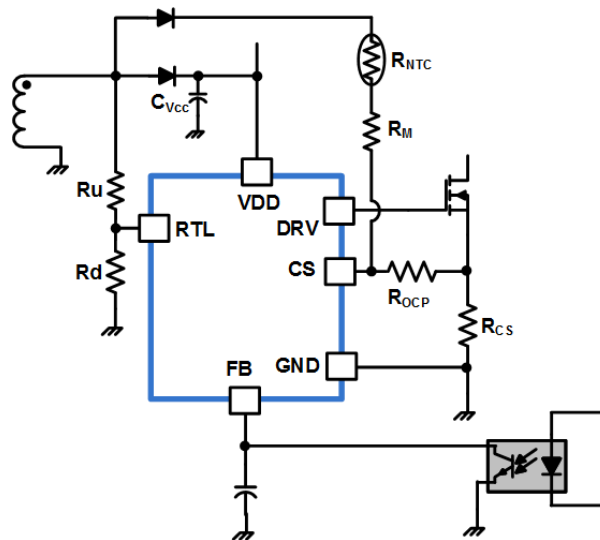


Fig.9

**DRV**

The driving capability of CL1850 is around 450mA, which can support power rate around 60~70W, and it is limited the maximum duty-cycle below 80% to avoid the transformer saturation.

Typically, the threshold of MOSFET is about 20V, and the maximum clamp voltage of CL1850 is 14V to prevent breakdown of MOSFET.

**Complete Protection**

CL1850 integrates various kind of protection to make sure operation safety.

**VDD OVP (Over Voltage Protection)**

The maximum ratings of the CL1850 are around 30V. To prevent the VDD enter breakdown condition, CL1850 series are integrated with OVP function on VDD pin. Whenever the VDD voltage is higher than the  $V_{OVP}$  threshold, the output gate drive circuit will be turn-off simultaneously and the power MOSFET is turn-off until the next UVLO(on) cycle.

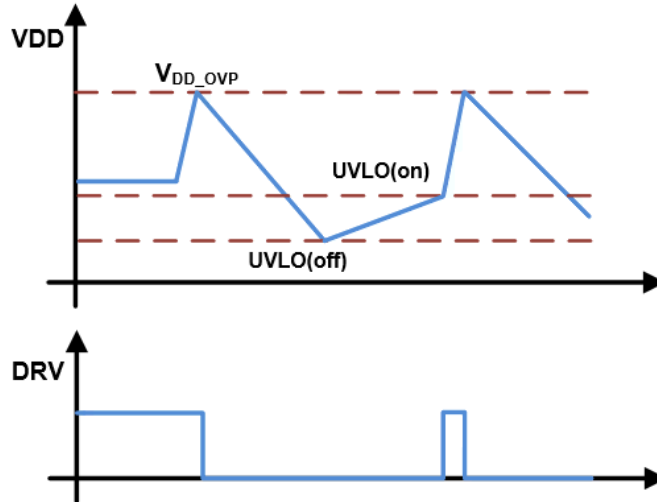


Fig.10

**SCP (Short Circuit Protection)**

A resistive divider between Aux winding and GND is used to monitor output voltage. When output circuit is short, therefore, as  $V_{RTL}$  is lower than 0.8V during date off region, then  $V_{TH\_UVP}$  is triggered,

CL1850 is to enable UVP function in order to reduce input power

**SDSP, Secondary Diode Short Protection**

After short circuit of 2<sup>nd</sup> side schottky, the inductance current is too low to discharge completely caused by lower output voltage, and then it will continues to increasing to induce abnormal saturation of transformer during LEB timing, therefore, higher peak current induce serious high  $V_{ds}$  to damage MOSFET.

CL1850 detects the inductance current through the resistance,  $R_{cs}$ , of CS pin, and will trigger protection (latch or hiccup) when  $V_{cs}$  higher than 0.85V and sustains 2cycle timing.

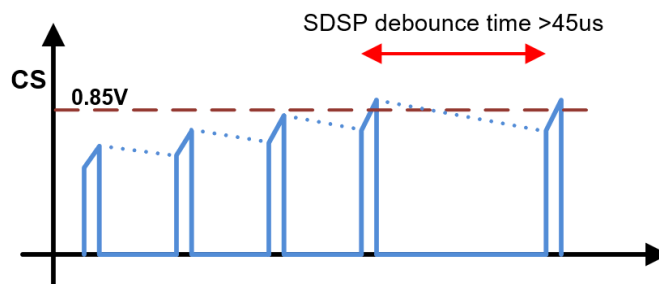


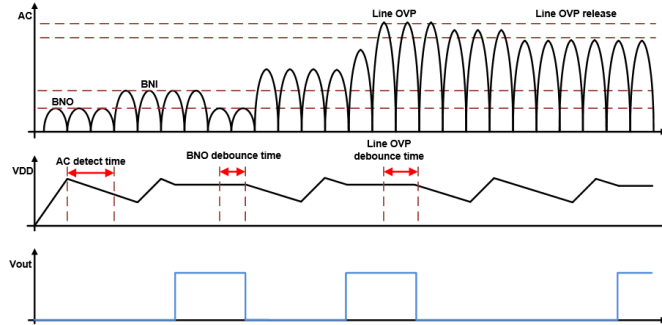
Fig.11

**AC, Brown-in/out & Line OVP**

IN2P083B provides real detection of AC line through AC pin connected directly to AC line. When the VDD of IN2P083B reaches UVLO\_ON , it is into the state of AC detection ,and sustains a delay time  $T_{ADC}$  .This AC pin is used to program the AV over and under voltage level through a resistive divider ( $R_{a1}/R_{a2}$ ).

If  $V_{ac}$  is lower than below  $V_{BNI}$  or higher than  $V_{LNOVP\_HYS}$ , it will turn-off the output till next cycle to check the condition is removed or not. Even after it turn-off, this pin is continues to detect line status. If  $V_{ac}$  is lower than below  $V_{BNO}$  or higher

than  $V_{LNOVP}$  for the timing  $T_{BNO}$  and  $T_{LNOVP}$ , it will be turn-off, and re-start again. Please refers to fig12.

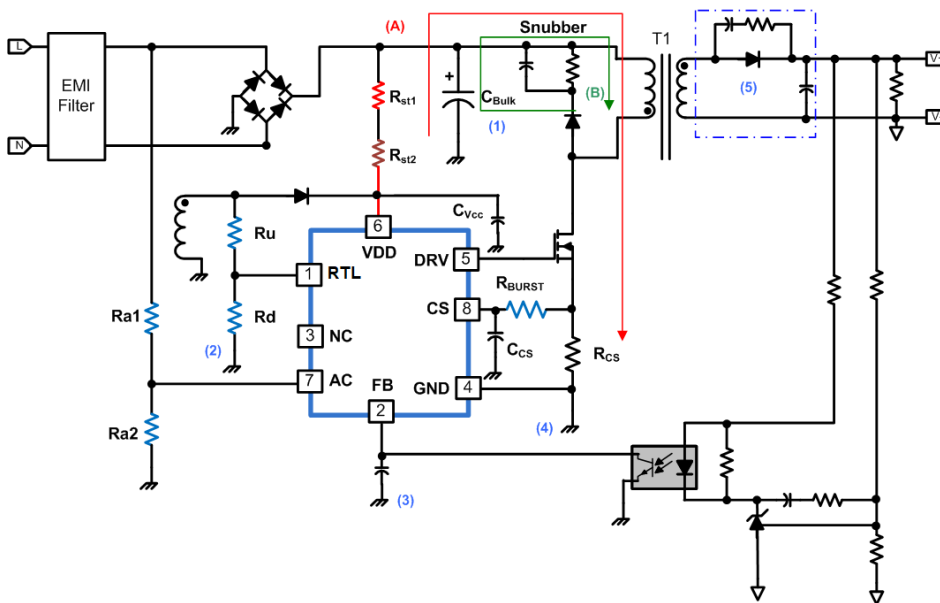


**Fig.12**

**Layout Guide line**

Better layout plan can reduce unknow noise no matter signal or EMI, please refer to the list below :

- **Big current path** : A&B (Area 1) area are high frequency current loop, line to line is as close as possible, and avoid near low voltage control area
- **Low voltage area** : R divider need to be as near FB\_Pin as possible.
- **Secondary Side Schottky** : routing as close as possible
- **Grounding** : (2).(3) and (4) grounding separated with each other, and end connects to (1) ground.
- **RTL** : Ru & Rd as close as possible to avoid noise coupling to trigger OVP.



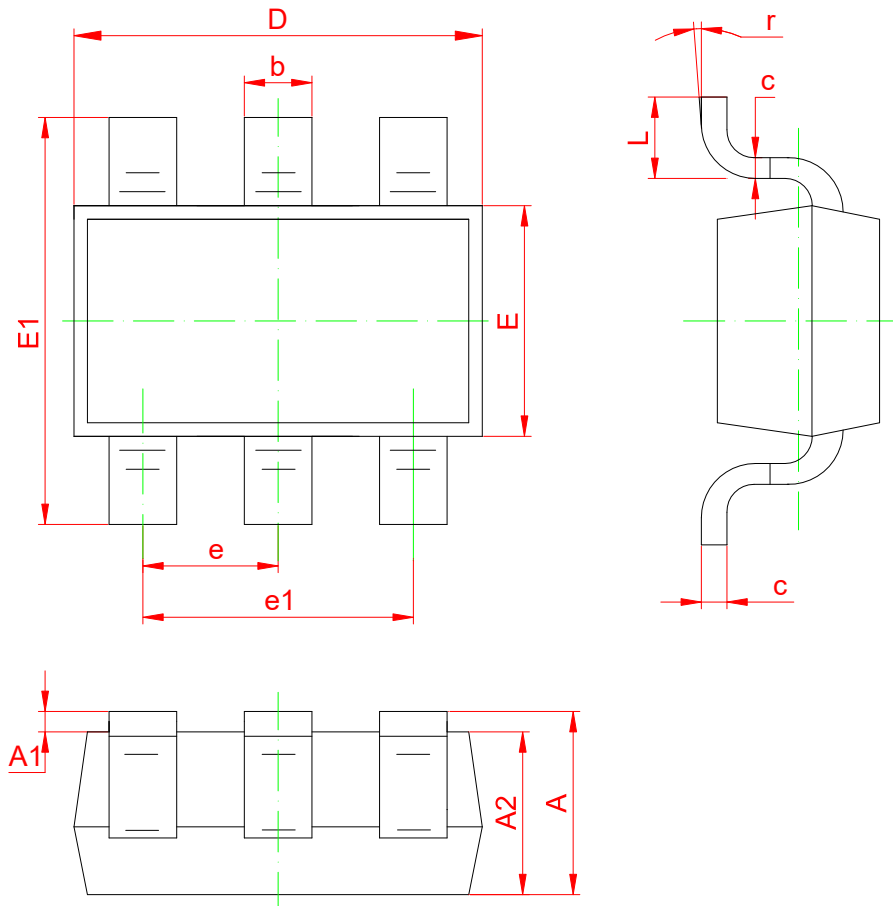
**Fig.13**

保护功能 Table 1: Complete Protection

Issue	Protection		Pin	Protection Conditions
1st	V-Sense	VDD OVP	VDD	VDD > 28V
1st	V-Sense	VDD UVLO Off	VDD	VDD < 7.5V
1st	V-Sense	Brown In Fail	AC	VAC < 0.85
1st	V-Sense	Brown out	AC	VAC > 0.75V
1st	V-Sense	Line OVP	AC	VAC > 3.0V
1st	V-Sense	T1 Aux gnd open	RTL	RTL UVP trigger
1st	V-Sense	MOS short/Gate to GND	RTL	RTL UVP trigger
1st	V-Sense	CS pin open	CS	VCS > 0.7V after 4 cycles
1st	RTL	RTL upper R open	RTL	RTL UVP : after soft-start RTL < 0.85V & FB > 4V
1st	RTL	RTL upper R short	RTL	RTL OVP : RTL > 3V & FB > 4V
1st	RTL	RTL down side open	RTL	RTL OVP : RTL > 3V & FB > 4V
1st	RTL	RTL down-side short	RTL	RTL UVP : after soft-start time RTL < 0.85V & FB > 4V
2nd	SDSP	2nd side Schottky short	CS	VCS > 0.85V after 4 cycles
2nd	SCP	Output short	RTL	1. 12ms blank time during start-up 2. after 4 cycles 3. RTL UVP = 0.8V & FB > 4V trigger
2nd	OVP	Output OVP	RTL	VRTL compares to 3V through the resistance divider
1nd	OCP	OCP	CS	Hi/Low line OCP external adjust , Max current limit CS = 0.7V
2nd	OLP	OLP	CS	CS > 0.5V
2nd	Short before power on		RTL	1. 12ms blank time at start-up 2. after 4 cycles 3. RTL UVP = 0.8V & FB > 4V trigger
2nd	Short after power on		RTL	1. after 4 cycles 2. RTL UVP = 0.8V & FB > 4V trigger
IC	Chip OTP			chip OTP at 150 C

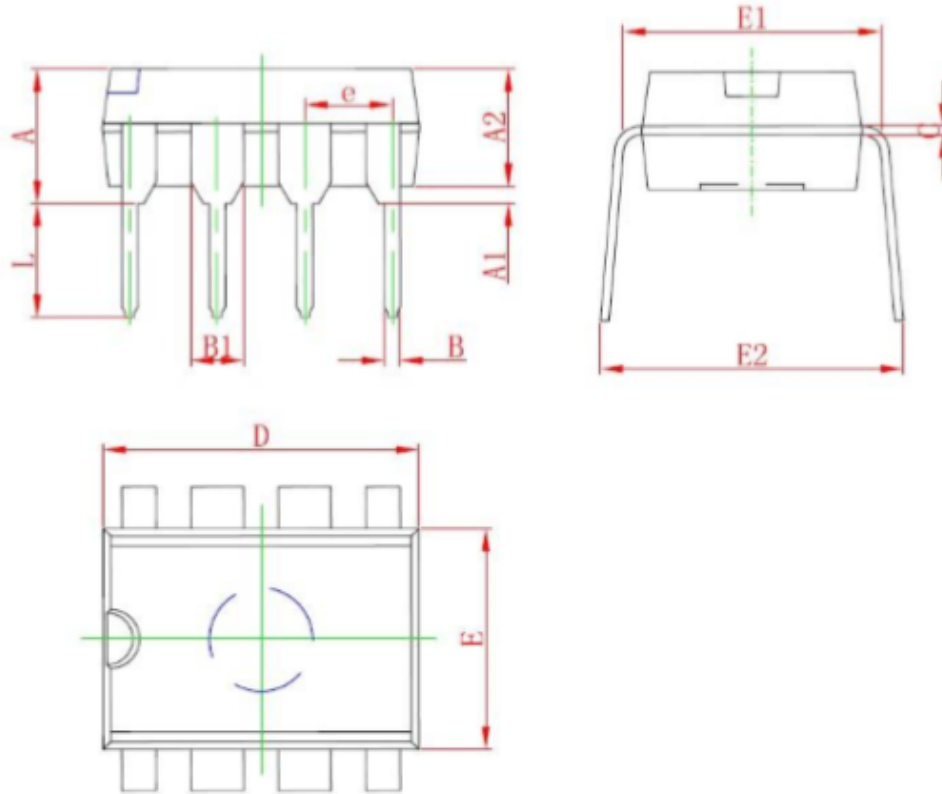


**Package Information: SOT-23-6L**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
r	0°	8°	0°	8°

**Package Information: DIP8**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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