# CHIPLINK DUAL N-Channel Enhancement Mode Power MOSFET

## Description

The LX8205A combines advanced trench technology to provide excellent $R_{DS(ON)}$. This device is suitable for use as battery protection or a load switch application.

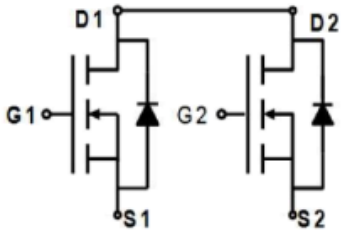
## Features

- $V_{DS}$=20V, $I_D$=5A
  $R_{DS(ON)}$ <29mΩ@VDS=4.5V
  $R_{DS(ON)}$ <34mΩ@VDS=2.5V
- High power and current handing capability
- Common drain configuration for design simplicity
- Termination is Lead-free and RoHS Compliant

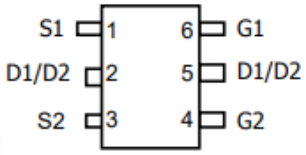
## Applications

- Battery protection switch
- Load switch

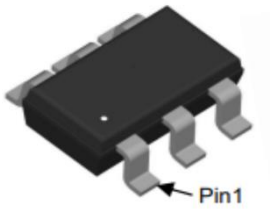
## Schematic Diagram




## Pin Assignment




## SOT23-6 Package




## Maximum Ratings($T_A$=25℃ unless otherwise noted)

| Parameter | Symbol | Maximum | Units |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | $V_{GS}$ | ±12 | V |
| Continuous Drain Current | $I_D$ | 5 | A |
| Pulsed Drain Current[B] | $I_{DM}$ | 20 | A |
| Maximum Power Dissipation[A] | $P_D$ | 1.25 | W |
| Junction and Storage Temperature Range | $T_J$, $T_{STG}$ | -55 To 150 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{QJA}$ | 100 | ℃/W |

## Electrical Characteristics ($T_A$=25℃unless otherwise specified)

| Parameter | Symbol | Test conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250uA | 20 | | | V |
| Gate-Threshold Voltage | $V_{th(GS)}$ | $V_{DS}$= $V_{GS}$, $I_D$=250 uA | 0.5 | 0.7 | 1.2 | V |
| Gate-body Leakage | IGSS | $V_{DS}$=0V, $V_{GS}$=±10V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | IDSS | $V_{DS}$=20V, $V_{GS}$=0V | | | 1 | uA |
| Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$ =4.5V, $I_D$ =2.5A | | 20 | 29 | mΩ |
| | | $V_{GS}$ =2.5V, $I_D$ =2.0A | | 27 | 34 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=5V, $I_D$ =1.0A | | 18 | | s |
| **Dynamic Characteristics** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10V, $V_{GS}$ =0V, F=1MHz | | 418 | | pF |
| Output Capacitance | $C_{oss}$ | | | 82 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 70 | | |
| **Switching Capacitance** | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$= 10V, $R_L$=2.9Ω $V_{GS}$ = 4.5V, $R_{GEN}$=3Ω | | 4.2 | | nS |
| Turn-on Rise Time | $t_r$ | | | 19.8 | | nS |
| Turn-off Delay Time | $t_{d(off)}$ | | | 22.6 | | nS |
| Turn-off Fall Time | $t_f$ | | | 20 | | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10V, $I_D$=2A, $V_{GS}$ =4.5V | | 10.5 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 5 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | 2.5 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage | $V_{SD}$ | $V_{GS}$ =0V, $I_D$=5A | | | 1.2 | V |
| Diode Forward Current | Is | | | | 2.0 | A |

**Notes:**

A. The Power dissipation $P_D$ is based on $T_{J(MAX)}$=150℃, using≤10s junction-to ambient thermal resistance.

B. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃.Ratings are based on low frequency and duty cycles to keep initial $T_J$=25℃.

C. The Static characteristics in Figures are obtained using 〈300 μs pulses, duty cycle 2% max.

## Typical Electrical and Thermal Characteristics

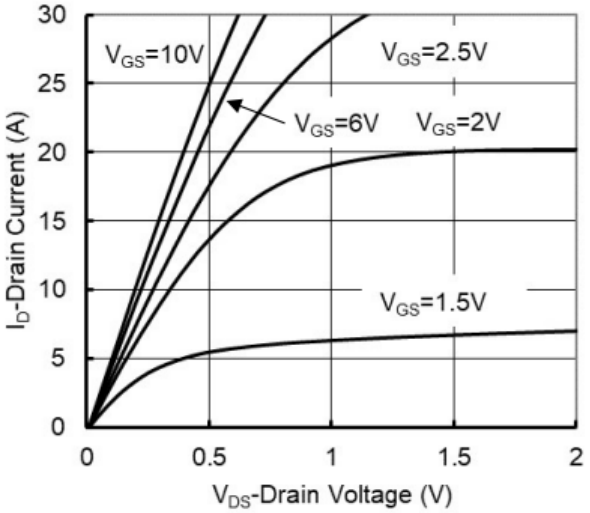



**Figure1. Output Characteristics**

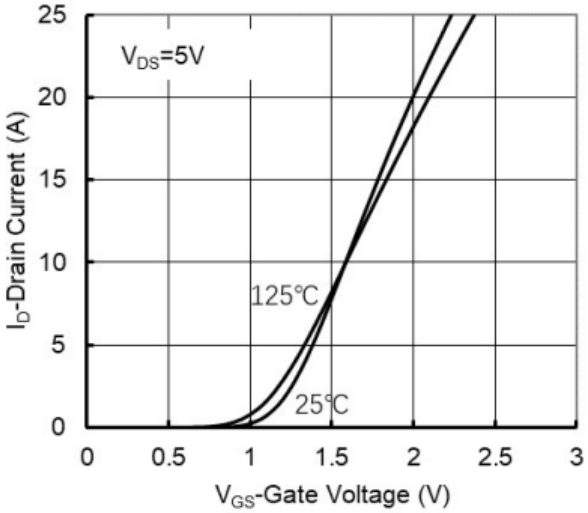



**Figure2. Transfer Characteristics**

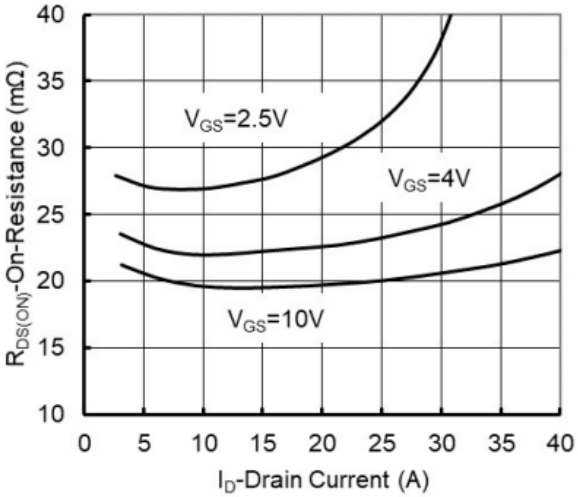



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**

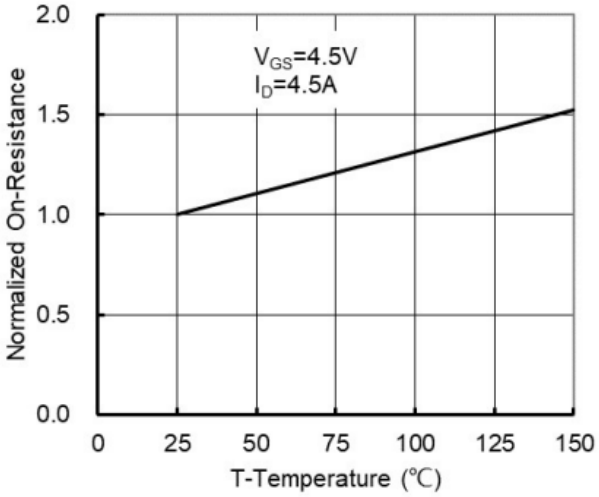



**Figure 4: On-Resistance vs. Junction Temperature**

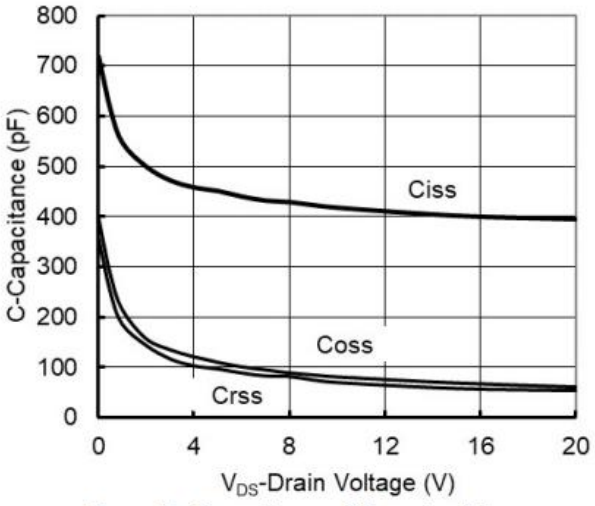



**Figure5. Capacitance Characteristics**

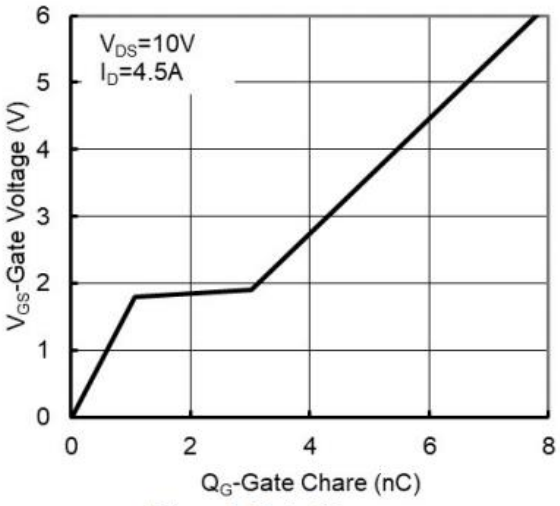



**Figure6. Gate Charge**

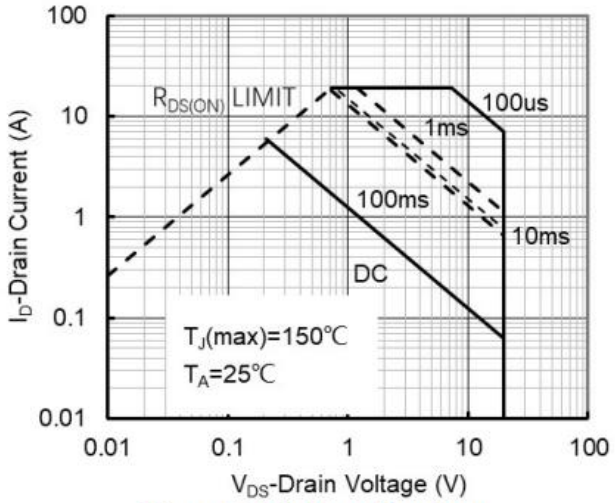



**Figure7. Safe Operation Area**

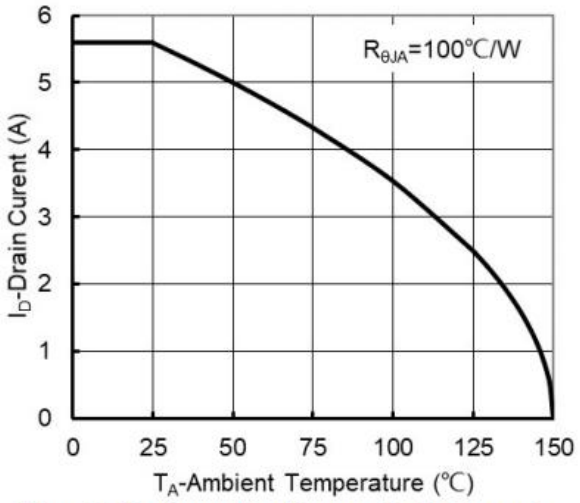



**Figure8. Maximum Continuous Drain Current vs Ambient Temperature**

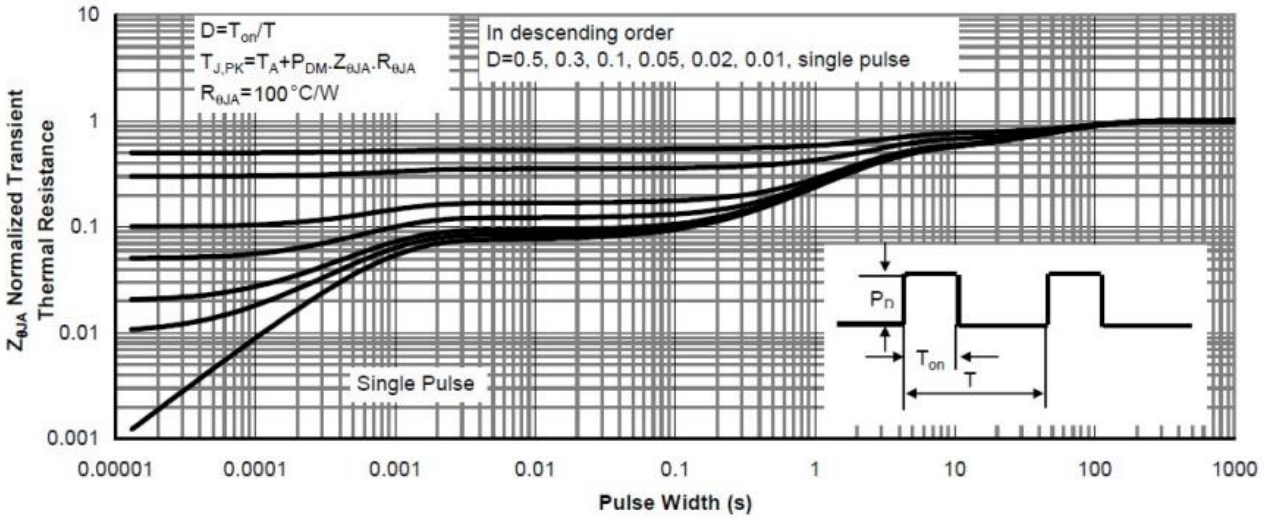



**Figure9. Normalized Maximum Transient Thermal Impedance**

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