

ME7660 Charge Pump DC-DC Voltage Converter

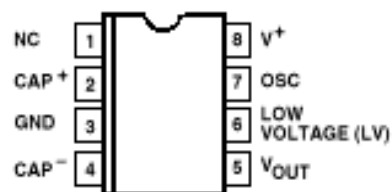
Introduction

Me7660 is a charge pump dc-to-dc voltage converter using AL-gate CMOS technology and optimization design. It converts a +1.5V to +10V input to a corresponding -1.5V to -10V output using only two external capacitors, eliminating inductors and their associated cost, size and EMI. The on-board oscillator operates at a nominal frequency of 10KHZ. Operation below 10 KHZ (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground.

Features:

- ✧ Converts +5V Logic supply to $\pm 5V$
- ✧ Wide input voltage range: 1.5V~10V
- ✧ Efficient voltage conversion: 99.9%
- ✧ Good power efficiency: 98%
- ✧ Low power supply: 50uA @5V_{in}
- ✧ Easy to use: only two external capacitors required
- ✧ 8-pin DIP and 8-pin small outline packages are available
- ✧ Compatible with RS232 negative power supply standard
- ✧ High ESD protection: up to 3kV
- ✧ No Dx diode needed for high voltage operation

Pin Configuration

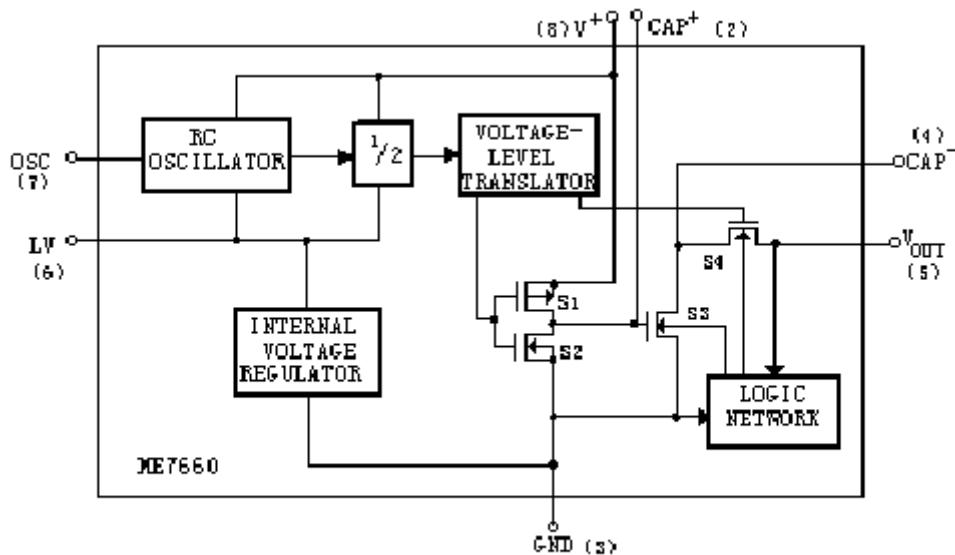


Packages: 8-pin DIP and 8-pin SOIC

Pin Description

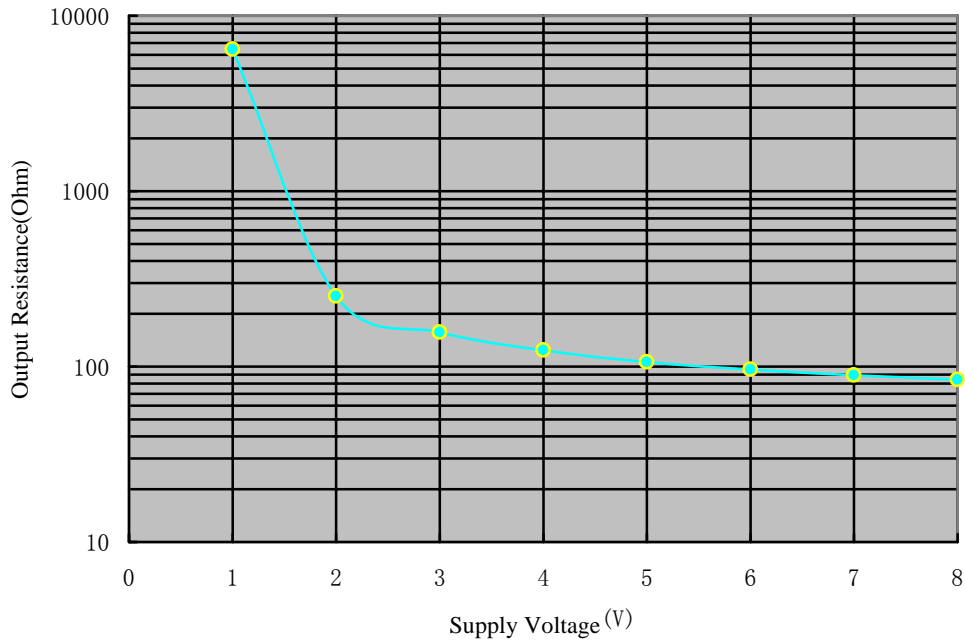
Pin No.	Symbol	Description
1	NC	No connection
2	CAP ⁺	Connecting external capacitor (+) pin
3	GND	Ground Pin
4	CAP ⁻	Connecting external capacitor (-) pin
5	V _{out}	Voltage output pin
6	Low Voltage	Low voltage selection pin
7	OSC	Connecting oscillation capacitor pin
8	V ⁺	Power supply pin

Functional Block Diagram

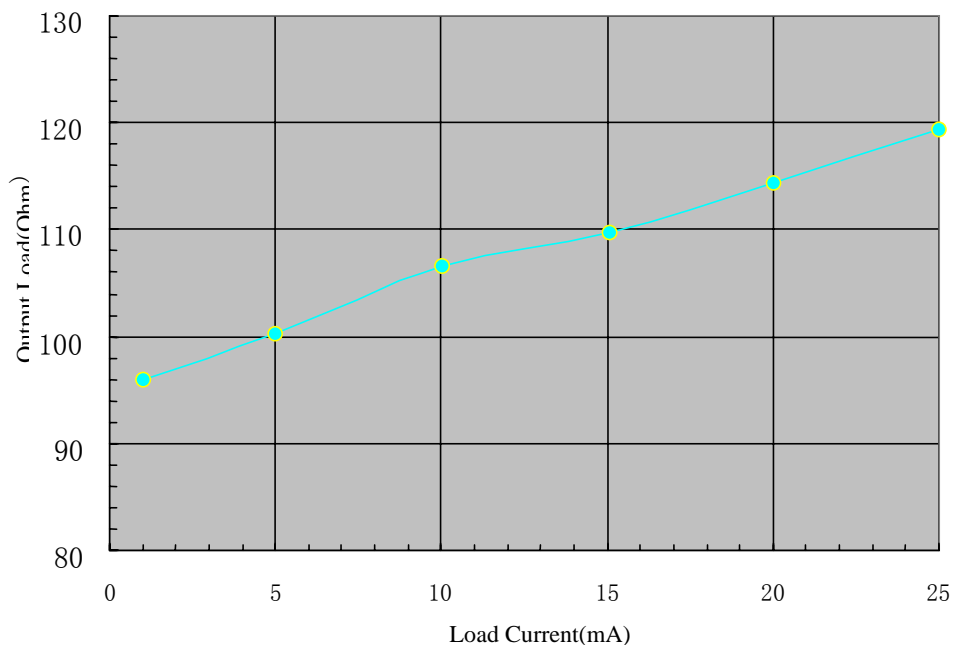


Typical Performance Characteristics

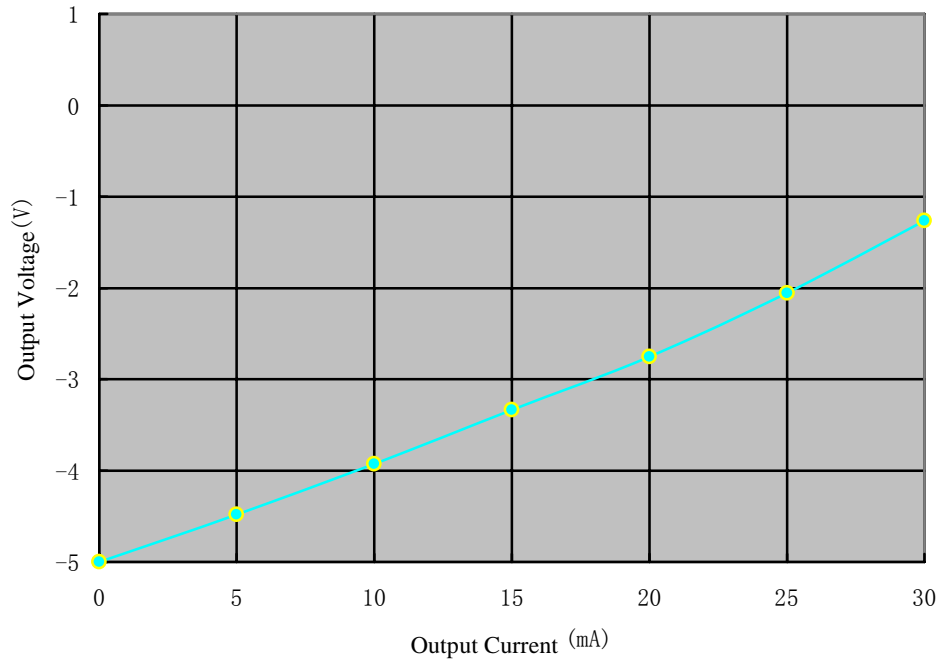
Output Resistance vs. Supply Voltage



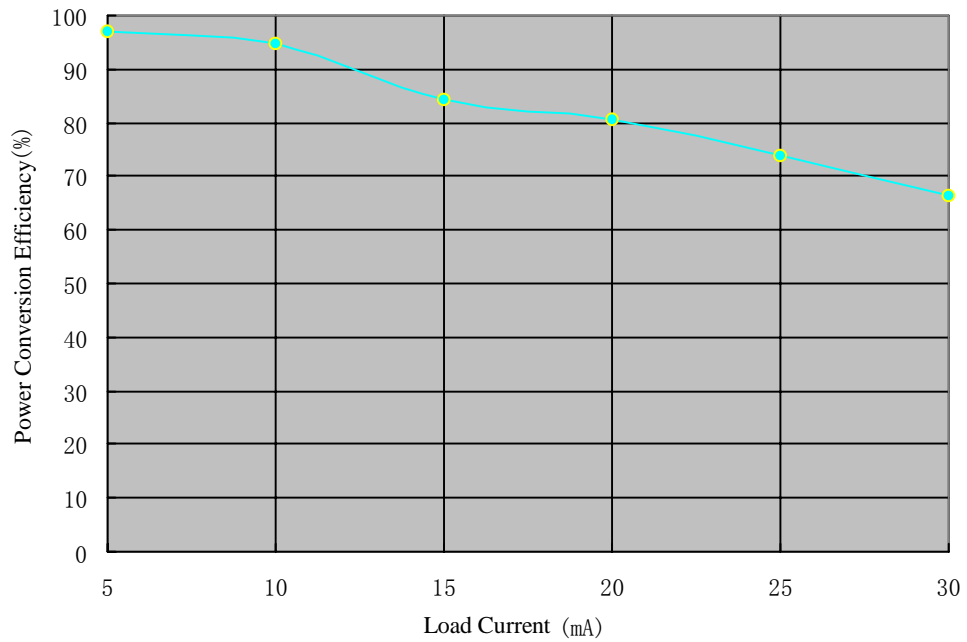
Output Load vs. Load Current^(V⁺=+5V)



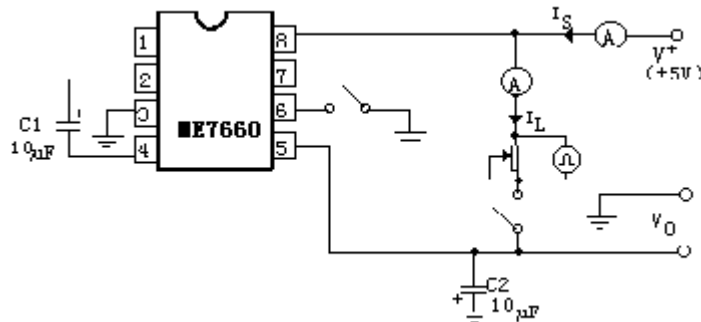
Output Voltage vs. Output Current ($V^+=+5V$)



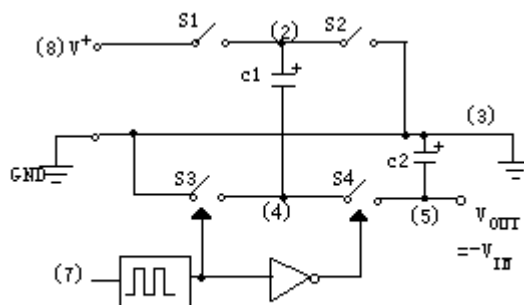
Power Conversion Efficiency vs. Load Current ($V^+=+5V$)



Testing Circuit



Detailed Description



ME7660 together with two external capacitors C1、C2 complement a voltage Inverter. Capacitor C1 is charged to a voltage V^+ , for the first half cycle when switches S1 and S3 are closed (while switches S2 and S4 are open during this half cycle); During the second half cycle of operation, switches S2 and S4 are closed, with S1 and S3 open, thereby shifting capacitor C2 negatively to $-V^+$.

The voltage regulator portion of the chip is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation.

Theoretical Power Efficiency Considerations

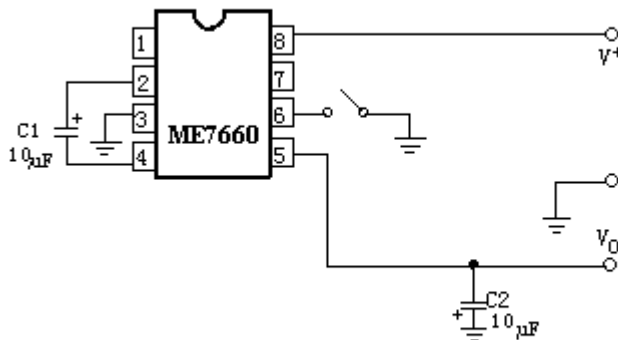
In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

- ✧ The drive circuitry consumes no power.
- ✧ The output switches have extremely low ON resistance and no offset when operation.
- ✧ The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

Notes:

- ✧ Supply voltage should not exceed maximum rating;
- ✧ Do not connect LV terminal to GND for supply voltages greater than 3.5V;
- ✧ Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods;
- ✧ Polarized capacitors should be connected as the figure above.

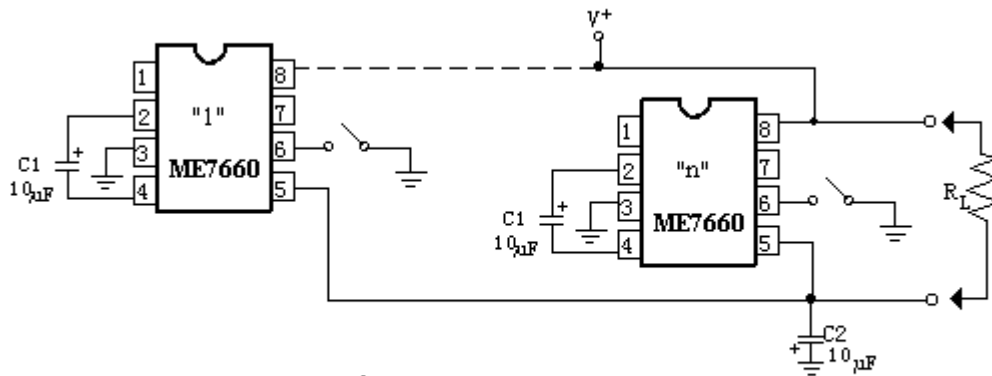
Typical Application Circuit



Above figure is the basic application circuit to provide a negative supply from -1.5V ~ -10V while a positive supply from +1.5V ~ +10V is available. When $V^+ = +5V$, the output resistance is about $100\ \Omega$; The output voltage is $-4V$ while the load current is 10mA.

Paralleling Circuit

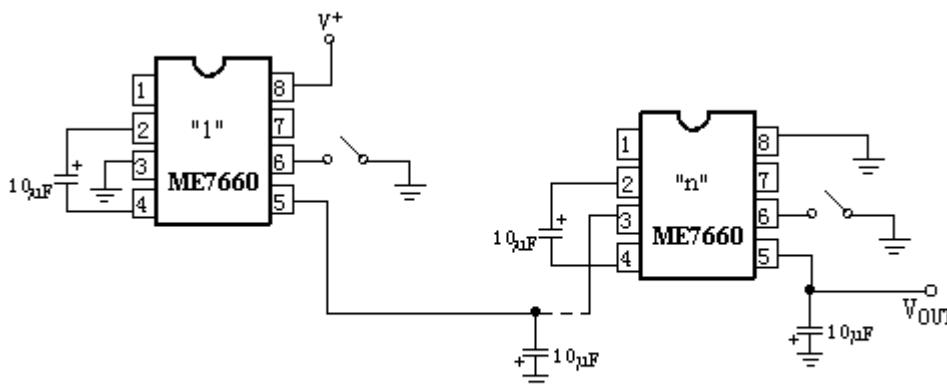
ME7660 may be paralleled to reduce output resistance (see the figure below).



$$R_{out} = R_{out}(\text{of Me7660})/n(\text{number of devices})$$

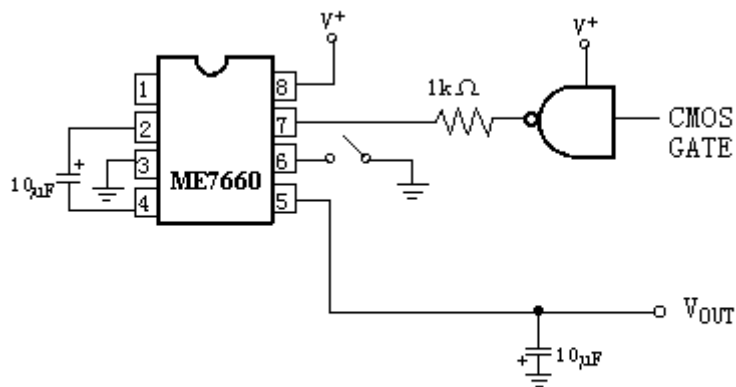
Cascading Devices

Me7660 may be cascaded as shown below to produce larger negative output voltage. However, due to the finite efficiency of each device, the number of practical cascading devices are limited. The output resistance is approximately n of a single chip resistance (n is the number of devices cascaded.)



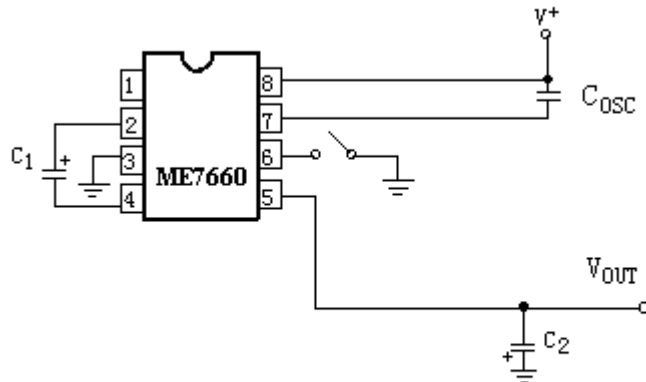
Adjusting Oscillator Frequency

In some applications due to noise, it may be desirable to increase the oscillator frequency. This can be achieved by overdriving the oscillator from an external clock as shown in the figure below.



The external clock output should connect a $1\text{k}\Omega$ resistor to prevent device latch-up. Besides, the pump frequency will be half of the clock frequency because of the internal circuit.

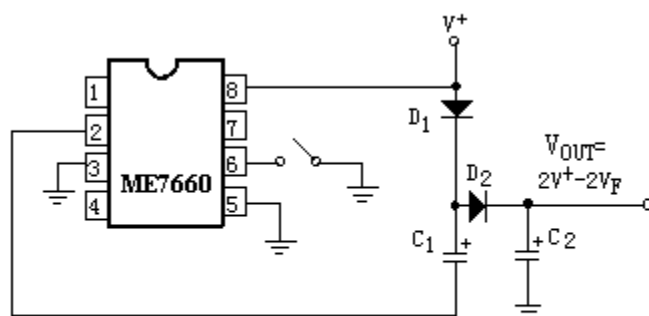
To increase the conversion efficiency, the oscillator frequency may be lowered by connecting a capacitor from pin 7 and pin 8 as shown below.



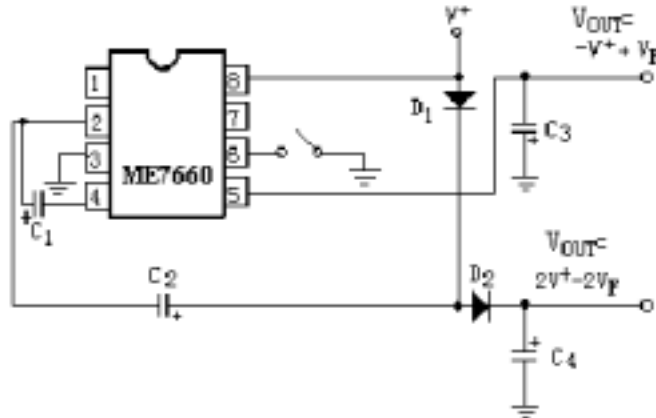
This reduces the switching losses. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump and reservoir capacitors. So, the values of C_1 and C_2 should be increased by the same factor that the frequency has been reduced.

Voltage Multiplication

ME7660 may be applied to achieve positive voltage multiplication using the circuit shown in the figure below.



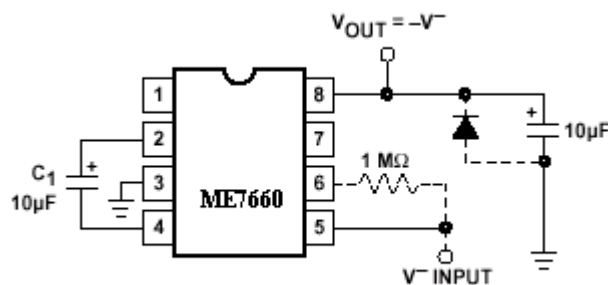
Combined Negative Voltage Conversion and Positive Supply Multiplication



In the figure, C1、C3 are the pump and reservoir capacitors respectively for the generation of the negative voltage; C2、C4 are the pump and reservoir capacitors respectively for the multiplied positive voltage. When +5V supply is provided, +9V and -5V can be generated.

Positive Voltage Multiplication/Conversion

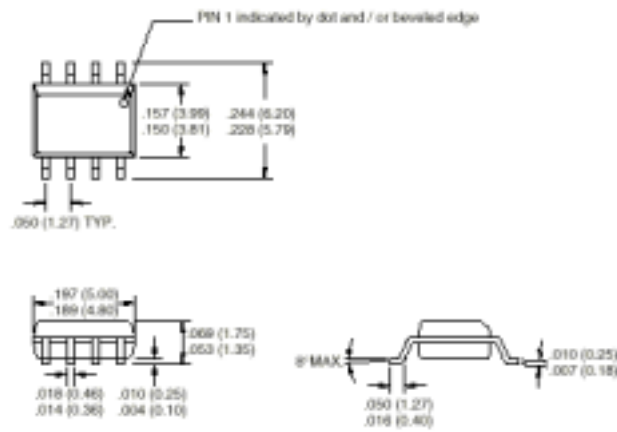
Since the switches that allow the charge pumping operation are bi-directional, the charge transfer can be performed backwards as easily as forwards. Following figure shows ME7660 transforming -5V to +5V (or +5V to +10V, etc.).The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated.



Package Dimensions

8-Pin SOIC

Dimensions: inches (mm)



8-Pin Plastic DIP

