

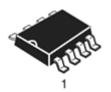
N-Channel MOSFET MEM2306

General Description

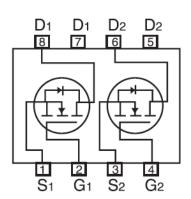
MEM2306SG Series Dual N-channel enhancement mode field-effect transistor produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications, and low power dissipation.

Features

- 20V/5A,
 - $R_{DS(ON)} = 29 \text{m}\Omega \otimes V_{GS} = 3.85 \text{V}, I_D = 5 \text{A}$
- High Density Cell Design For Ultra Low On-Resistance
- surface mount package: SOP8



Pin Configuration



Typical Application

- Battery management
- power management
- Portable equipment
- Low power DC to DC converter.
- Load switch
- LCD adapter

Absolute Maximum Ratings

Par	Symbol	Ratings	Unit	
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current	T _A =25℃	I _D	5	Α
Pulsed Drain Current ^{1,2}		I _{DM}	30	Α
Total Power Dissipation	T _A =25℃	D	1.3	١٨/
	T _A =70°C	P_D	1.0	W
Operating Temperature Range		T_{Opr}	150	$^{\circ}$
Storage Temperature Range		T _{stg}	−65/150	$^{\circ}$



Thermal Characteristics

Parameter		Symbol	Ratings	Unit
Thermal Resistance,	Stoody State	D	62.5	°C/W
Junction-to-Ambient ³	Steady-State	R _{θJA}	62.5	C/VV

Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Туре	Max	Unit	
		Static Character	istics				
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V _{GS} =0V, I _D =250μA	20	23		V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS},$ $I_{D}=250\mu A$	0.5	0.72	1	V	
Gate-Body Leakage	I _{GSS}	$V_{DS}=0V$, $V_{GS}=12V$		5	100	nA	
		V _{DS} =0V, V _{GS} =-12V		-7	-100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	V _{DS} =16V V _{GS} =0V		1.8	1000	nA	
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =4.5V,I _D =6A			23	mΩ	
		V _{GS} =3.85V,I _D =5A			25	mΩ	
		V _{GS} =2.5V,I _D =4A			35	mΩ	
Forward Transconductance	g _{FS}	$V_{DS} = 10 \text{ V}, I_{D} = 6A$	6	20		S	
Source-drain (diode forward) voltage	V_{SD}	V _{GS} =0V,I _S =1.5A		0.8	1	V	
		Dynamic Characte	ristics				
Input Capacitance	Ciss	V 0.V		1120	1500		
Output Capacitance	Coss	$V_{DS} = 8 V$,		480	630	- pF	
Reverse Transfer Capacitance	Crss	$V_{GS} = 0 V,$ f = 1 MHz		110	160		
		Switching Characte	eristics				
Turn-On Delay Time	td(on)	$V_{DD} = 10 \text{ V},$ $RL = 10\Omega$		25	60		
Rise Time	tr	I _D =1 A,		60	140	ns	
Turn-Off Delay Time	td(off)	$V_{GEN} = 4.5 \text{ V},$		60	140		
Fall-Time	tf	Rg = 6 Ω		50	60		
Total Gate Charge	Qg	V _{DS} = 10 V,		47	60		
Gate-Source Charge	Qgs	$V_{GS} = 4.5 \text{ V},$		6		nc	
Gate-Drain Charge	Qgd	$I_D = 6 A$		8			



Typical Performance Characteristics:

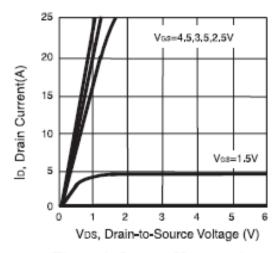


Figure 1. Output Characteristics

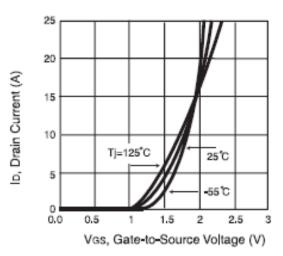
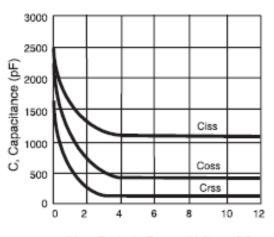


Figure 2. Transfer Characteristics



VDS, Drain-to Source Voltage (V)

0.06 Vas=4.5V Tj=125*C 0.04 0.03 0.03 25*C 0.00 0.01 0.00 0 5 10 15 20 ID, Drain Current(A)

Figure 4. On-Resistance Variation with Drain Current and Temperature



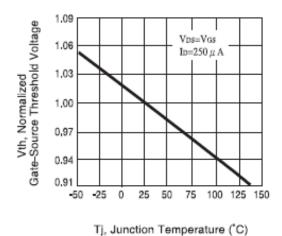
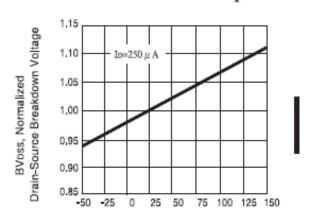


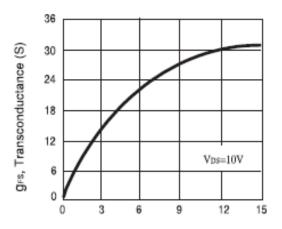
Figure 5. Gate Threshold Variation with Temperature



Tj, Junction Temperature (°C)

Figure 6. Breakdown Voltage Variation with Temperature





lps, Drain-Source Current (A)

Figure 7. Transconductance Variation with Drain Current

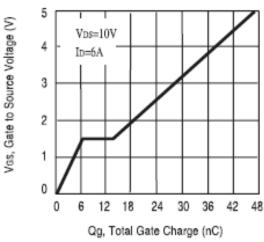


Figure 9. Gate Charge

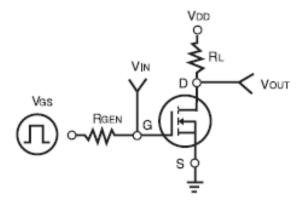
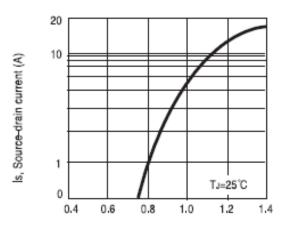


Figure 11. Switching Test Circuit



Vsp, Body Diode Forward Voltage (V)

Figure 8. Body Diode Forward Voltage Variation with Source Current

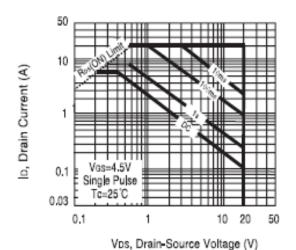


Figure 10. Maximum Safe Operating Area

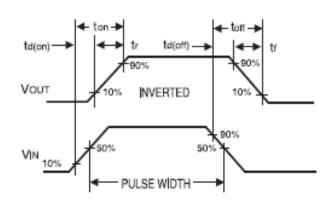


Figure 12. Switching Waveforms



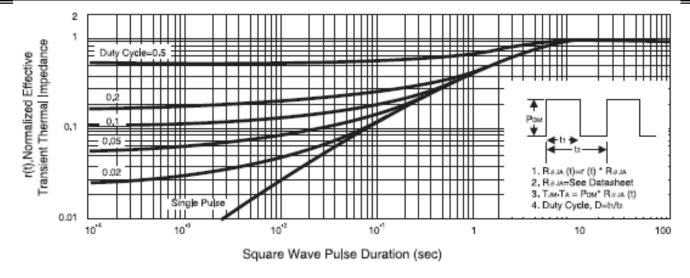
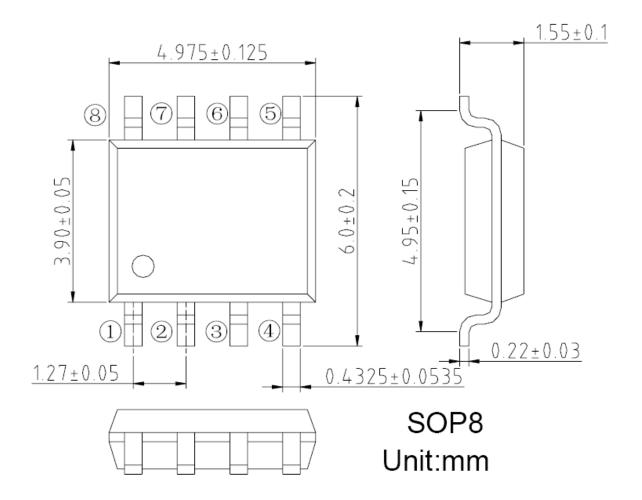


Figure 13. Normalized Thermal Transient Impedance Curve

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