

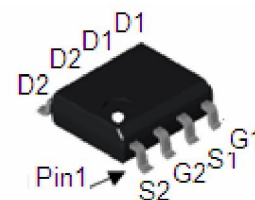
P-Channel MOSFET MEM2313

General Description

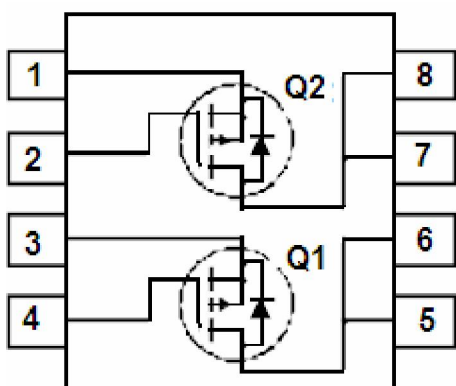
MEM2313SG Series Dual P-channel enhancement mode field-effect transistor, produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage .

Features

- I -30V/-6A
- $R_{DS(ON)}=52m @ V_{GS}=-10V, I_D=-6A$
- $R_{DS(ON)}=67m @ V_{GS}=-4.5V, I_D=-4A$
- I High Density Cell Design For Ultra Low On-Resistance
- I Surface mount package:SOP8



Pin Configuration



Typical Application

- I Power management
- I Load switch
- I Battery protection

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units	
Drain-Source Voltage	V_{DSS}	-30V	V	
Gate-Source Voltage	V_{GSS}	± 20	V	
Drain Current	I_D	$T_A=25$	-6	A
		$T_A=70$	-4	
Pulsed Drain Current ^{1,2}	I_{DM}	-30	A	
Total Power Dissipation	P_d	$T_A=25$	1.3	W
		$T_A=70$	0.8	
Operating Temperature Range	T_{Opr}	150		
Storage Temperature Range	T_{stg}	-65/150		

Thermal Characteristics

Parameter		Symbol	Ratings	Units
Thermal Resistance, Junction-to-Ambient ³	Steady-State	R_{JA}	62.5	$^{\circ}W$

Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-34		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.3	-2	V
Gate-Body Leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=20V$		0.8	100	nA
		$V_{DS}=0V, V_{GS}=-20V$		-0.8	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$		-3.5	-300	nA
Static Drain-Source On-Resistance	$R_{DS(ON)1}$	$V_{GS}=-10V, I_D=-6A$	33	52	65	m
	$R_{DS(ON)2}$	$V_{GS}=-4.5V, I_D=-4A$	50	67	80	m
Forward Transconductance	g_{FS}	$V_{DS} = -5 V, I_D = -5 A$		10		S
Drain-Source Diode Forward Current	I_S				-1.3	A
Source-drain (diode forward) voltage	V_{SD}	$V_{GS}=0V, I_D=-1A$		-0.8	-1.2	V
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS} = -15V,$ $V_{GS} = 0 V,$ $f = 1 MHz$		530		pF
Output Capacitance	C_{oss}			140		
Reverse Transfer Capacitance	C_{rss}			70		
Switching Characteristics						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 V,$ $I_D=-1 A,$ $V_{GEN} = -10 V,$ $R_g = 6$		8	15	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall-Time	t_f			10	17	
Total Gate Charge	Q_g	$V_{DS} = -15 V,$ $V_{GS} = -5V,$ $I_D = -5A$		10	15	nC
Gate-Source Charge	Q_{gs}			2.2		
Gate-Drain Charge	Q_{gd}			2		

- 1、 Pulse width limited by Max. junction temperature.
- 2、 Pulse width <300us , duty cycle <2%.
- 3、 Surface Mounted on FR4 Board, t < 10 sec.

Typical Performance Characteristics

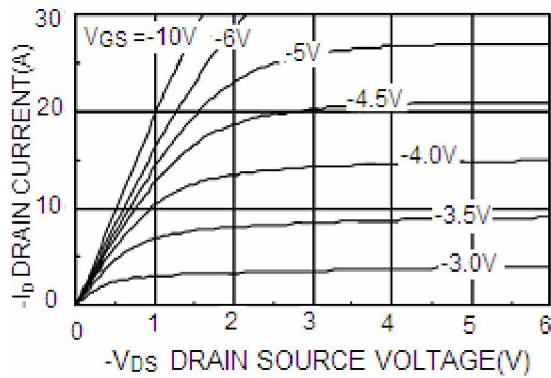


Fig.1 On-region characteristics

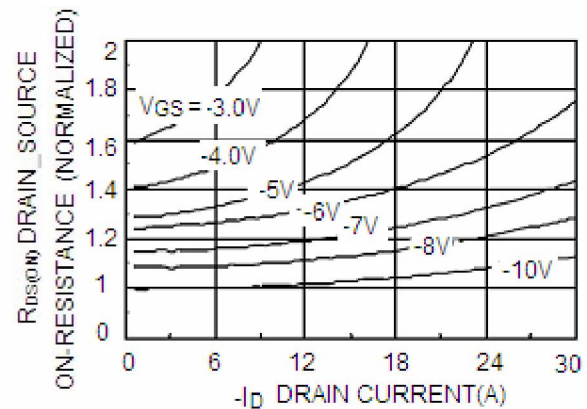


Fig.2 On-resistance variation with drain current and gate voltage

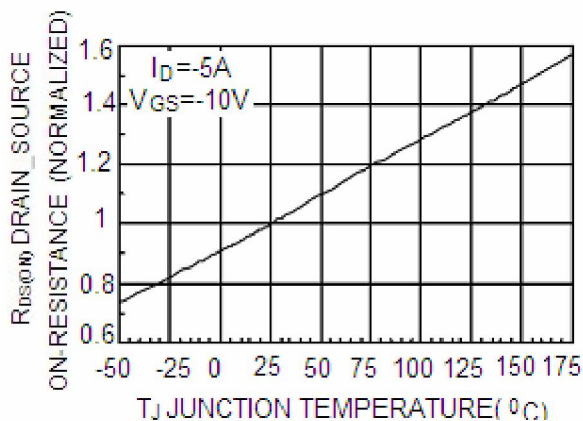


Fig.3 On-resistance variation with temperature

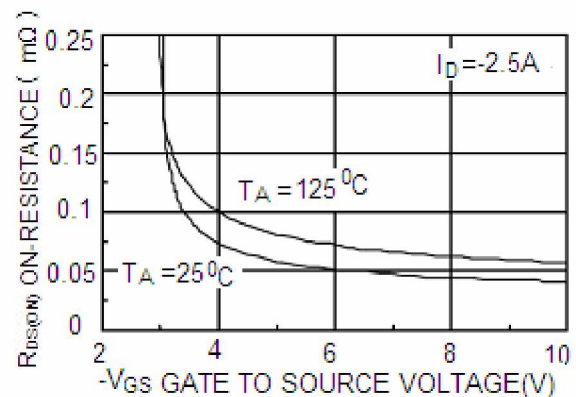


Fig.4 On-resistance variation with gate-to source voltage

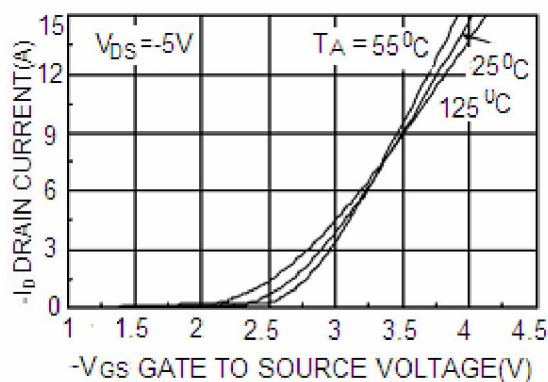


Fig.5 Transfer characteristics

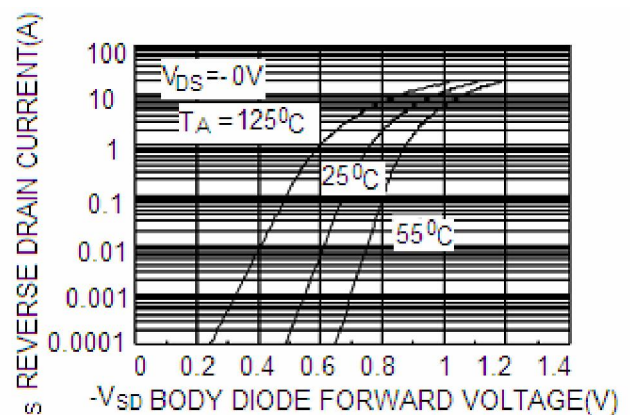


Fig.6 Body diode forward voltage variation with source current and temperature

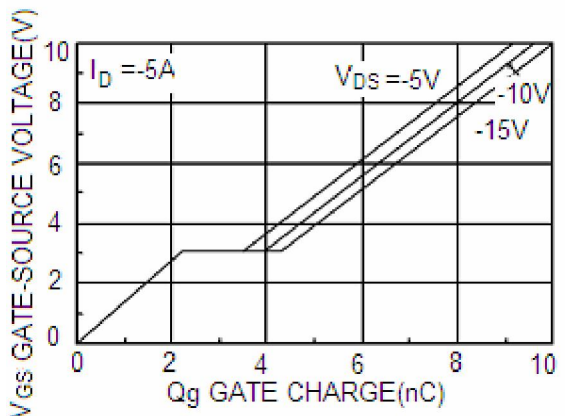


Fig.7 Gate charge characteristics

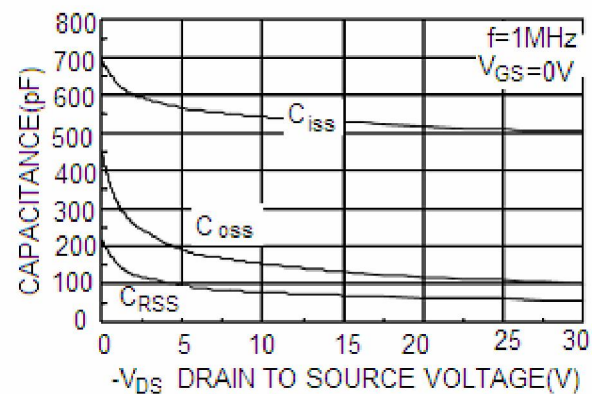


Fig.8 Capacitance characteristics

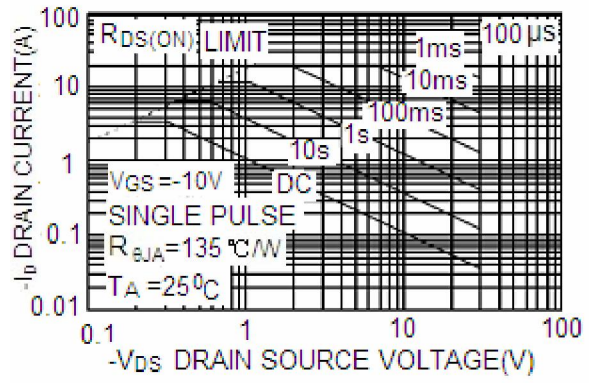


Fig.9 Maximum safe operating area

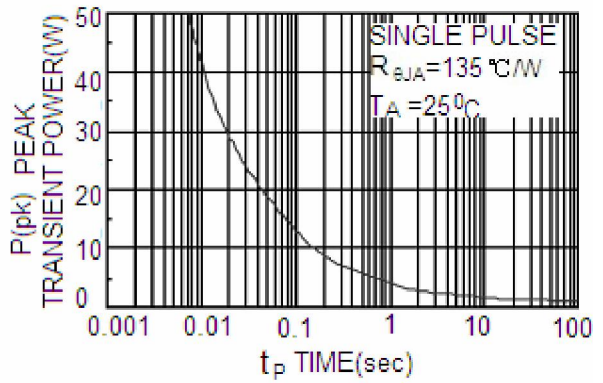


Fig.10 Single pulse maximum power dissipation

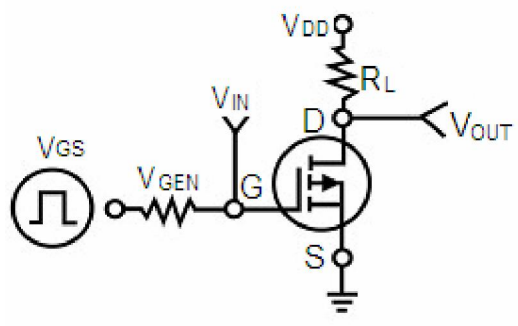


Fig.11 Switching test circuit

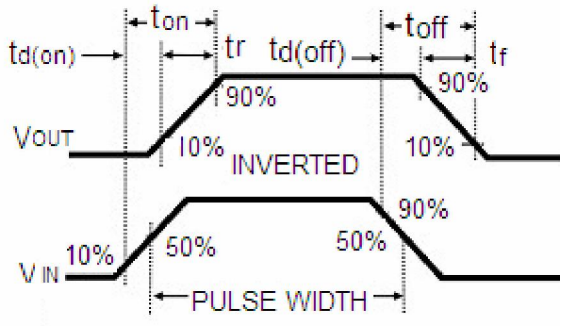


Fig.12 Switching waveforms

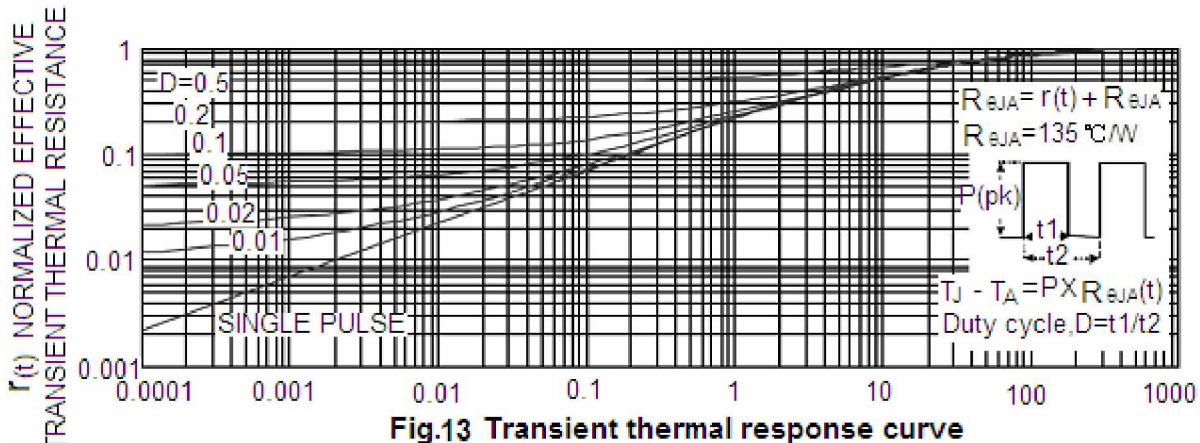


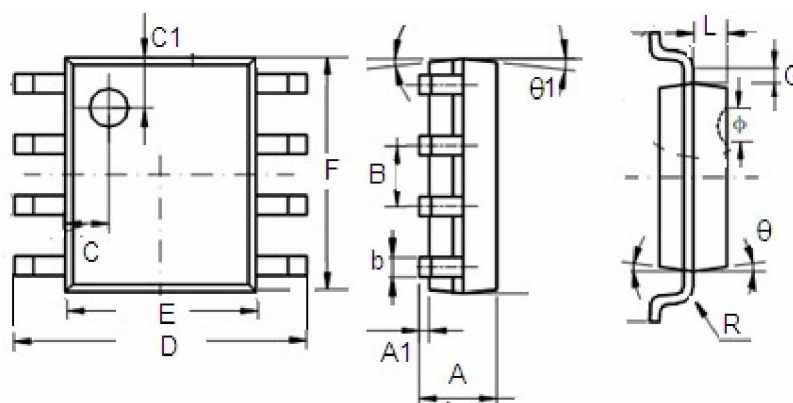
Fig.13 Transient thermal response curve

Thermal characterization performed using the conditions described in note IC.

Transient thermal response will change depending the circuit board design.

Package Information

• SOP8



Character	Dimension (mm)		Dimension (Inches)	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.1	0.3	0.004	0.012
B	1.27(Typ.)		0.05(Typ.)	
b	0.330	0.510	0.013	0.020
C	0.9(Typ.)		0.035(Typ.)	
C1	1.0(Typ.)		0.039(Typ.)	
D	5.8	6.2	0.228	0.244
E	3.800	4.000	0.150	0.157
F	4.7	5.1	0.185	0.201
L	0.675	0.725	0.027	0.029
G	0.32(Typ.)		0.013(Typ.)	
R	0.15(Typ.)		0.006(Typ.)	
	0.8(Typ.)		0.031(Typ.)	
theta1	7°		7°	
theta	8°		8°	