LITEON OPTOELECTRONICS

Data Sheet

Photocouplers
LTV-316J series

LTV-316J series

5.0 Amp Gate Drive Optocoupler with Integrated (V_{CE}) Desaturation Detection and Fault Status Feedback

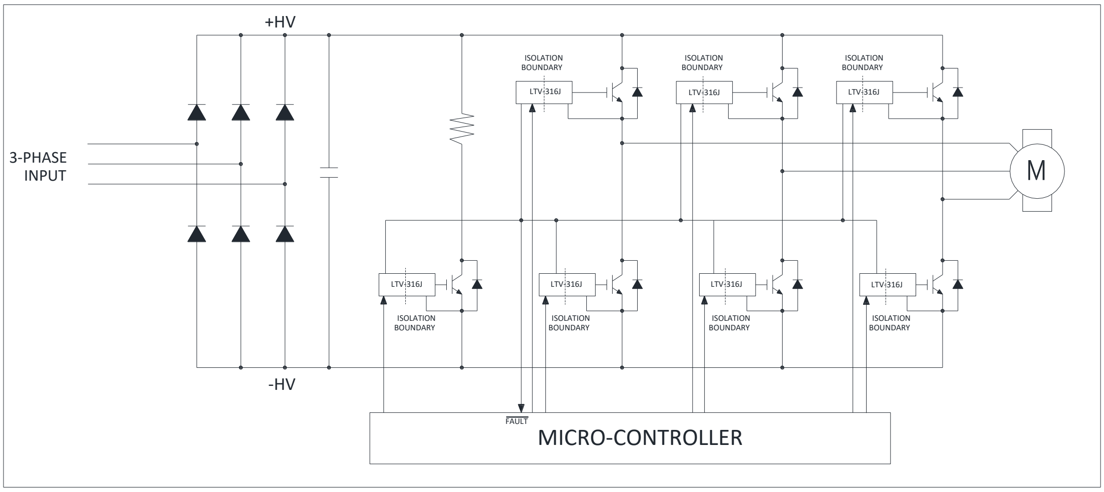
1. DESCRIPTION

The LTV-316J contains an AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. LTV-330J is ideally suited for driving power IGBTs and MOSFET used in motor control inverter applications. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 150 A. For IGBTs with higher ratings, the LTV-316J can be used to drive a discrete power stage which drives the IGBTs gate. The LTV-316J has an insulation voltage of V_{IORM} = 1414 V_{PEAK}.The Optocoupler operational parameters are guaranteed over the temperature range from -40ºC ~ +100ºC.

1.1 Features

- 5.0 A maximum peak output current
- Drive IGBTs up to I_C = 150 A, V_{CE} = 1200 V
- Optically isolated, FAULT status feedback
- CMOS/TTL compatible
- 15 kV/us minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- Integrated fail-safe IGBT protection
  – Desat (VCE) detection
  – Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide V_{CC} operating range: 15 to 30 Volts (V_{CC})
- Guaranteed performance over temperature -40ºC ~ +100ºC.
- Safety approval: UL/ cUL 1577, 5000 Vrms/1 min
  VDE DIN EN60747-5-5, V_{IORM} = 1414 Vpeak
  CQC GB4943.1-2011/ GB8898-2011 (meet Altitude up to 5000m)

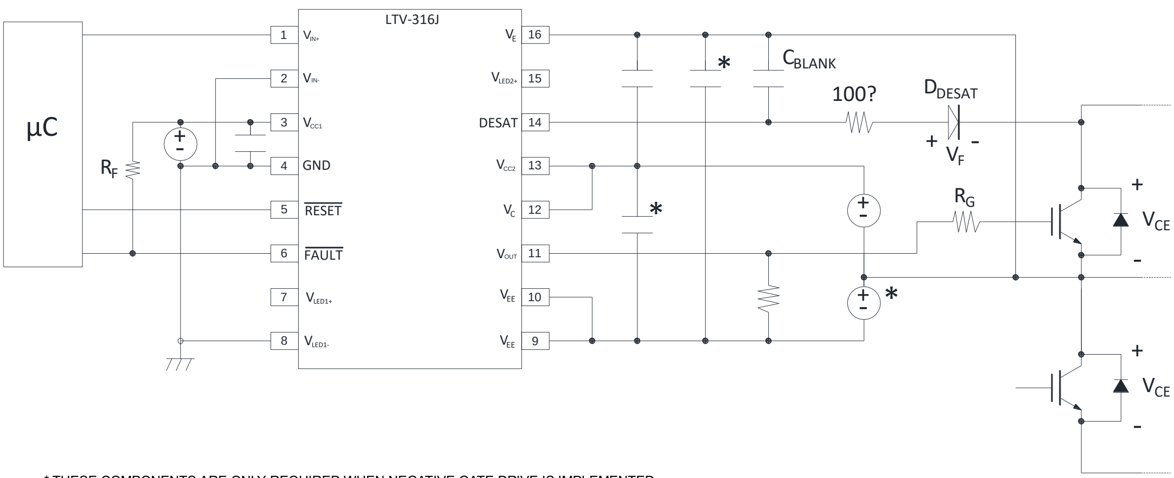
1.2 Fault Protected IGBT Gate Drive



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.

1.3 Fault Protected IGBT Gate Drive

The LTV-316J is an easy-to-use, intelligent gate driver which makes IGBT VCE fault protection compact, affordable, and easy-to-implement. Features such as user configurable inputs, integrated V_{CE} detection, under voltage lockout (UVLO), "soft" IGBT turn-off and isolated fault feed back provide maximum design flexibility and circuit protection.



* THESE COMPONENTS ARE ONLY REQUIRED WHEN NEGATIVE GATE DRIVE IS IMPLEMENTED.

1.4 Description of Operation during Fault Condition

1. DESAT terminal monitors the IGBT V_{CE} voltage through D_{DESAT}.
2. When the voltage on the DESAT terminal exceeds 7 volts, the IGBT gate voltage (V_{OUT}) is slowly lowered.
3. $\overline{FAULT}$ output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.

V_{IN+}	V_{IN-}	UVLO (V_{CC2}-V_E)	Desat Condition Detected on Pin14	Pin6(FAULT) Output	VOUT
X	X	Active	X	X	Low
X	X	X	Yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not Active	No	High	High

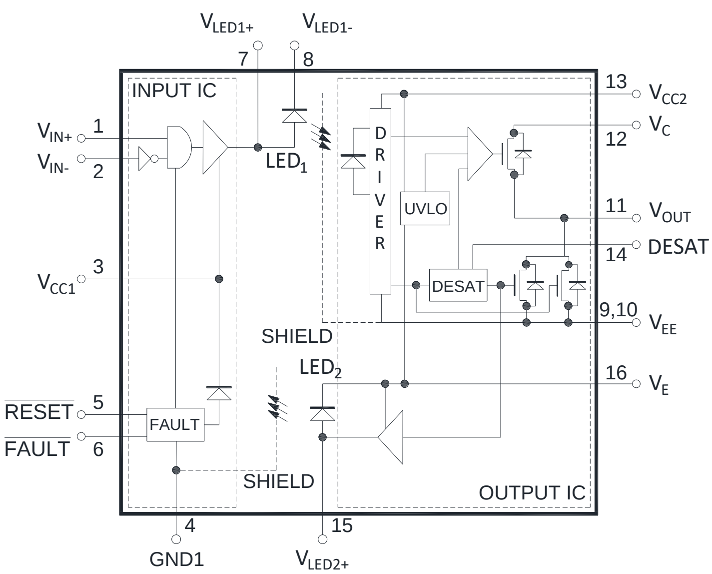
1.5 Output control

The outputs (V_{OUT} and $\overline{FAULT}$) of the LTV-316J are controlled by the combination of V_{IN}, UVLO and a detected IGBT Desat condition. As indicated in the below table, the LTV-316J can be configured as inverting or non-inverting using the V_{IN+} or V_{IN-} inputs respectively. When an inverting configuration is desired, V_{IN+} must be held high and V_{IN-} toggled. When a non-inverting configuration is desired, V_{IN-} must be held low and V_{IN+} toggled. Once UVLO is not active (V_{CC2} - V_E > V_{UVLO}), V_{OUT} is allowed to go high, and the DESAT (pin 14) detection feature of the LTV-316J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{UVLO+} > 11.6 V, DESAT will remain functional until V_{UVLO-} < 12.4 V. Thus, the DESAT detection and UVLO features of the LTV-316J work in conjunction to ensure constant IGBT protection.

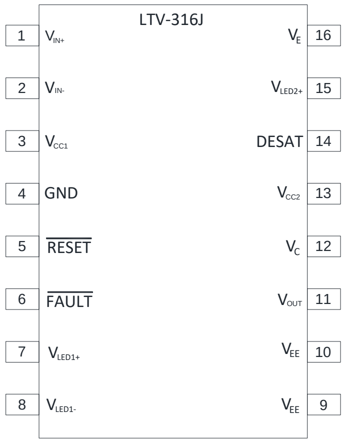
1.6 Product Overview Description

The LTV-316J is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit with fault protection and feed-back into one SO-16 package. TTL input logic levels allow direct interface with a microcontroller, and an optically iso-lated power output stage drives IGBTs with power ratings of up to 150 A and 1200 V. A high speed internal optical link minimizes the propagation delays between the microcon-troller and the IGBT while allowing the two systems to opera-te at very large common mode voltage differences that are common in industrial motor drives and other power switching applications. An output IC provides local protection for the IGBT to prevent damage during overcurrents, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in “watchdog” circuit monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages.This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of a discrete design. Two light emitting diodes and two integrated circuits housed in the same SOP-16 package provide the input control circuitry, the output power stage, and two optical channels. The input Buffer IC is designed on a bipolar process, while the output Detector IC is designed manufactured on a high voltage BiCMOS/Power DMOS process. The forward optical signal path, as indicated by LED1, transmits the gate control signal. The return optical signal path, as indicated by LED2, transmits the fault status feedback signal. Both optical channels are completely controlled by the input and output ICs respectively, making the internal isolation boundary transparent to the microcontroller.Under normal operation, the input gate control signal directly controls the IGBT gate through the isolated output detector IC. LED2 remains off and a fault latch in the input buffer IC is disabled. When an IGBT fault is detected, the output detector IC immediately begins a “soft” shutdown sequence, reducing the IGBT current to zero in a controlled manner to avoid potential IGBT damage from inductive overvoltages. Simultaneously, this fault status is transmitted back to the input buffer IC via LED2, where the fault latch disables the gate control input and the active low fault output alerts the microcontroller.During power-up, the Under Voltage Lockout (UVLO) feature prevents the application of insufficient gate voltage to the IGBT, by forcing the LTV-316J’s output low. Once the output is in the high state, the DESAT (VCE) detection feature of the LTV-316J provides IGBT protection.

Thus, UVLO and DESAT work in conjunction to provide constant IGBT protection.



1.7 Pin description



Symbol	Description	Symbol	Description
V_{IN+}	Noninverting gate drive voltage output (V_{OUT}) control input.	V_E	Common (IGBT emitter) output supply voltage.
V_{IN-}	Inverting gate drive voltage output (V_{OUT}) control input.	V_{LED2+}	LED 2 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
V_{CC1}	Positive input supply voltage. (4.5 V to 5.5 V)	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 7 V while the IGBT is on, FAULT output is changed from a high impedance state to a logic low state within 5 μs.
GND1	Input Ground	V_{CC2}	Positive output supply voltage.
$\overline{\text{RESET}}$	FAULT reset input. A logic low input for at least 0.1 μs, asynchronously resets FAULT output highand enables VIN. Synchronous control of RESET relative to VIN is required. RESET is not affected by UVLO. Asserting RESET while VOUT is high does not affect VOUT.	V_C	Collector of output pull-up triple-darlington transistor. It is connected to VCC2 directly or through a resistor to limit output turn-on current.
$\overline{\text{FAULT}}$	Fault output. FAULT changes from a high impedance state to a logic low output within 5 μs of the voltage on the DESAT pin exceeding an internal reference voltage of 7 V. FAULT output remains low until RESET is brought low. FAULT output is an open collector which allows the FAULT outputs from all LTV-316Js in a circuit to be connected together in a "wired OR" forming a single fault bus for interfacing directly to the micro-controller.	V_{OUT}	Gate drive voltage output.
V_{LED1+}	LED 1 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)	V_{EE}	Output supply voltage.
V_{LED1-}	LED 1 cathode. This pin must be connected to ground.	V_{EE}	Output supply voltage.

1.8 Ordering Information

LTV-316J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part number	Package	Option Name	Customized Code	Tape & Reel	IEC/EN/DIN/EN 60747-5-5 (V_{PR} method b)	Quantity	Others
LTV-316J	SOP-16	-	-			45 per tube	
		-V			●		
		-TP1		●		850 per reel	Location at higher right of tape
		-TP1-V		●	●		

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

LTV316J-V to order product of SOP-16 Surface Mount package in Tube packaging(Quantity: 45pcs per tube) with IEC/EN/DIN EN 60747-5-5 Safety Approval (V_{PR} method b).

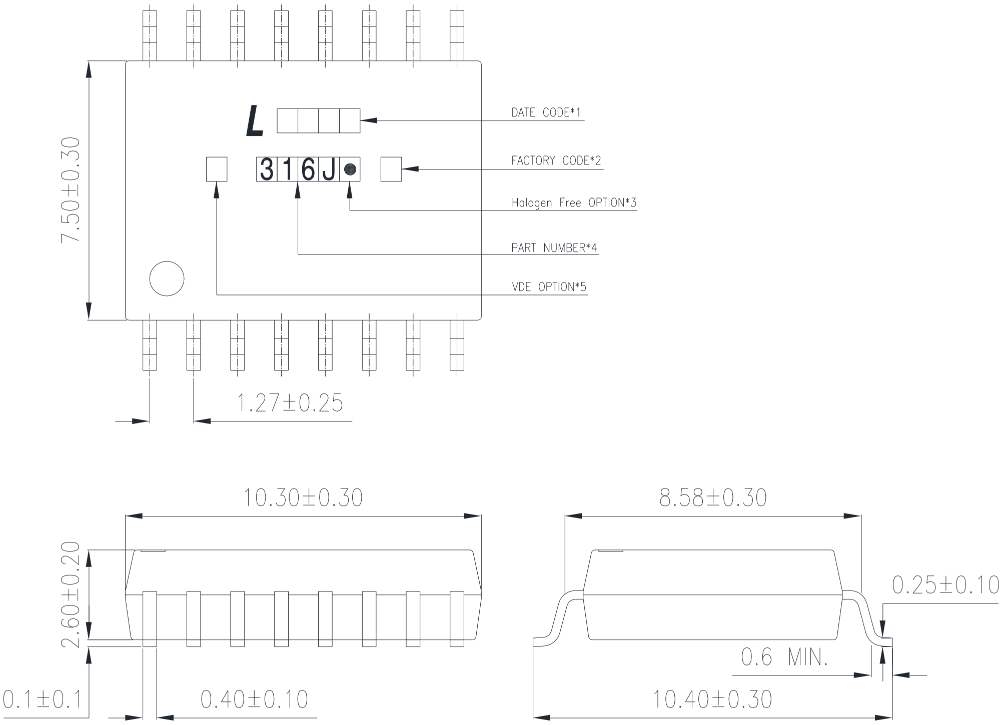
Example 2:

LTV316JTP1-V to order product of SOP-16 Surface Mount package in tape& reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval (V_{PR} method b).

Above option datasheets are available. Please contact your LITEON sales representative or authorized distributor for information.

2. PACKAGE DIMENSIONS

2.1 LTV-316J



Notes :

*1. Year date code and 2-digit work week.

*2. Factory identification mark(W :China-CZ).

*3. Halogen free option

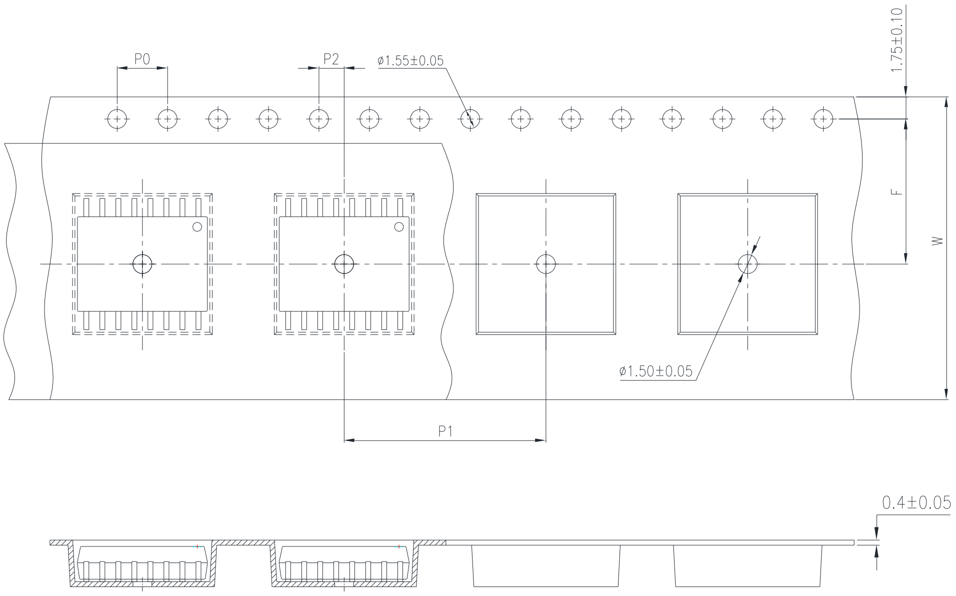
*4. Part number

*5. VDE option

Dimensions are in Millimeters and (Inches).

3. TAPING DIMENSIONS

3.1 LTV-316J-TP1



Description	Symbol	Dimension in mm (inch)
Tape wide	W	24±0.3 (0.94)
Pitch of sprocket holes	P_0	4±0.1 (0.15)
Distance of compartment	F	11.5±0.1 (0.452)
	P_2	2±0.1 (0.079)
Distance of compartment to compartment	P_1	16±0.1 (0.63)

3.3 Quantities Per Reel

Package Type	LTV-316J
Quantities (pcs)	850

4. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Description	Symbol	Characteristics	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage ≤ 150 V_{rms} for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms} for rated mains voltage ≤ 1000 V_{rms}		 I - IV I - IV I - IV I - III	
Climatic Classification		40/110/12	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input-to-Output Test Voltage, Method b *a, V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2651	V_{peak}
Input-to-Output Test Voltage, Method a *a, V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S,\ INPUT}$ $P_{S,\ OUTPUT}$	 175 400 1200	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	≥ 10^9	Ω

*a. Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5, for a detailed description.

*b. Ratings apply to all devices except otherwise noted in the Package column.

5. Insulation and Safety Related Specifications

Part number	Symol	LTV-316J	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

6. RATING AND CHARACTERISTICS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	T_{stg}	-55	+125	°C	—
Operating Temperature	T_{opr}	-40	+100	°C	—
Output IC Junction Temperature	T_J	—	125	°C	—
"High" Peak Output Current	$I_{OH(PEAK)}$	—	5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$	—	5	A	2
Positive Input Supply Voltage	V_{CC1}	-0.5	5.5	V	
FAULT Output Current	I_{FAULT}		8	mA	
Input Pin Voltages	V_{IN+}, V_{IN-} and $V_{\overline{RESET}}$	-0.5	V_{CC1}	V	
Total Output Supply Voltage	$(V_{CC2}-V_{EE})$	-0.5	35	V	—
Negative Output Supply Voltage	(V_E-V_{EE})	-0.5	15	V	
Positive Output Supply Voltage	$(V_{CC2}-V_E)$	-0.5	$35-(V_E-V_{EE})$	V	
Gate Drive Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC2}	V	—
Collector Voltage	V_C	$V_{EE}+5$	V_{CC2}	V	
DESAT Voltage	V_{DESAT}	V_E	V_E+10	V	
Power Dissipation	P_I		150	mW	—
Output Power Dissipation	P_O	—	600	mW	—
Lead Solder Temperature (10s)	T_{sol}	—	260	°C	—

Note: Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

6.2 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-40	100	ºC
Input Supply Voltage	V_{CC1}	4.5	5.5	V
Total Output Supply Voltage	$(V_{CC2}\text{-}V_{EE})$	15	30	V
Negative Output Supply Voltage	$(V_E\text{-}V_{EE})$	0	15	V
Positive Output Supply Voltage	$(V_{CC2}\text{-}V_E)$	15	30- $(V_E\text{-}V_{EE})$	V
Collector Voltage	V_C	V_{EE} + 6	V_{CC2}	V

6.3 ELECTRICAL OPTICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Figure	Note
Logic Low Input Voltages	V_{IN+L}, V_{IN-L} and $V_{\overline{RESET}L}$			0.8	V			
Logic High Input Voltages	V_{IN+H}, V_{IN-H} and $V_{\overline{RESET}H}$	2.0			V			
Logic Low Input Currents	I_{IN+L}, I_{IN-L} and $I_{\overline{RESET}L}$	-0.5			mA	V_{IN} = 0.4 V		
$\overline{FAULT}$ Logic Low Input Currents	$I_{\overline{FAULT}L}$	5.0			mA	V_{FAULT} = 0.4 V		
$\overline{FAULT}$ Logic High Input Currents	$I_{\overline{FAULT}H}$	-40			µA	V_{FAULT} = V_{CC1}		
High Level Output Current	I_{OH}	-2.5			A	V_{OUT} = V_{CC2} - 4 V		
		-5			A	V_{OUT} = V_{CC2} - 15 V		
Low Level Output Current	I_{OL}			2.5	A	V_{OUT} = V_{EE} + 2.5 V		
				5	A	V_{OUT} = V_{EE} + 15 V		
Low Level Output Current During Fault Condition	I_{OLF}	90		230	mA	V_{OUT} - V_{EE} = 14 V		

High Level Output Voltage	V_{OH}	V_{CC2} - 2	V_{CC2} - 1.5		V	I_{OUT} = -100 mA		
		V_{CC2} -1.5	V_{CC2} – 1			I_{OUT} = -650 µA		
				V_C		I_{OUT} = 0		
Low level Output Voltage	V_{OL}			0.5	V	I_{OUT} = 100 mA		
High Level Input Supply Current	I_{CC1H}			22	mA	V_{IN+} = V_{CC1} = 5.5 V, V_{IN-} = 0 V		
Low Level Input Supply Current	I_{CC1L}			11	mA	V_{IN+} = V_{IN-} = 0 V, V_{CC1} = 5.5 V		
Output Supply Current	I_{CC2}			5	mA	V_{OUT} open		
High Level Collector Current	I_{CL}			1	mA	I_{OUT} = 0mA		
Low Level Collector Current	I_{CH}			1.3	mA	I_{OUT} = 0mA		
				3.0		I_{OUT} = -650uA		
V_E High Level Supply Current	I_{EL}	-0.8	-0.5	0	mA	I_{OUT} = 0mA		
V_E Low Level Supply Current	I_{EH}	-0.5	-0.25	0	mA			
Blanking Capacitor Charging Current	I_{CHG}	-0.13		-0.33	mA	V_{DESAT} = 0 - 6 V		
		-0.18		-0.33	mA	V_{DESAT} = 0 - 6 V, T_A = 25°C - 100°C		
Blanking Capacitor Discharge Current	I_{DSCHG}	10			mA	V_{DESAT} = 7 V		
DESAT Threshold	V_{DESAT}	6.5	7.1	7.5	V	V_{CC2} – V_E > V_{UVLO-}		
UVLO Threshold	V_{UVLO+}	11.6		13.5	V	V_O > 5V, I_F = 10 mA		
	V_{UVLO-}			12.4	V	V_O < 5V, I_F = 10 mA		
UVLO Hysteresis	$UVLO_{HYS}$	0.4			V	(V_{UVLO+} - V_{UVLO-})		

6.4 SWITCHING SPECIFICATION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	100	220	500	ns	R_g = 10 Ω, C_g = 10 nF, f = 10 kHz, Duty Cycle = 50%		
Propagation Delay Time to Low Output Level	t_{PHL}	100	220	500	ns			
Pulse Width Distortion	PWD	-100	50	100	ns			
Propagation delay difference between any two parts or channels	PDD	-350		350	ns			
Output Rise Time (10 to 90%)	Tr		100		ns			
Output Fall Time (90 to 10%)	Tf		100		ns			
DESAT Sense to 90% V_O Delay	$t_{DESAT(90\%)}$			0.5	µs	R_g = 10 Ω, C_g = 10 nF,		
DESAT Sense to 10% V_O Delay	$t_{DESAT(10\%)}$			3	µs	V_{CC2} - V_{EE} = 30 V		
DESAT Sense to Low Level FAULT Signal Delay	$t_{DESAT(FAULT)}$			5	µs			17
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(LOW)}$		0.25		µs			18

$\overline{RESET}$ to High Level $\overline{FAULT}$ Signal Delay	$t_{\overline{RESET}(\overline{FAULT})}$	3		20	µs			19
$\overline{RESET}$ Signal Pulse Width	$PW_{\overline{RESET}}$	0.1			µs			
UVLO to V_{OUT} High Delay	t_{UVLO} ON			4.0	µs	V_{CC2} = 1.0 ms ramp		
UVLO to V_{OUT} Low Delay	t_{UVLO} OFF			6.0	µs			
Common mode transient immunity at high level output	|CMH|	15			kV/µs	T_A = 25°C, I_F = 10 mA, V_{CM} = 1500 V, V_{CC2} = 30 V,		
Common mode transient immunity at low level output	|CML|	15			kV/µs	T_A = 25°C, V_F = 0 V, V_{CM} = 1500 V, V_{CC2} = 30 V,		

6.5 PACKAGE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
Withstand Insulation Test Voltage	V_{ISO}	5000	—	—	V	RH ≤ 40-60%, t = 1min, T_A = 25°C,	1, 2
Input-Output Resistance	R_{I-O}	—	10^9	—	Ω	V_{I-O} = 500 V DC	1
Input-Output Capacitance	C_{I-O}	—	1.3	—	pF	f = 1MHz, T_A = 25°C	1

Note.1. According to UL1577, each Photocoupler is tested by applying an insulation test voltage 6000V_{RMS} for 1 second (leakage current less than 10uA). This test is performed before the 100% production test for partial discharge

Note.2. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.

7. TYPICAL PERFORMANCE CURVES & TEST CIRCUITS

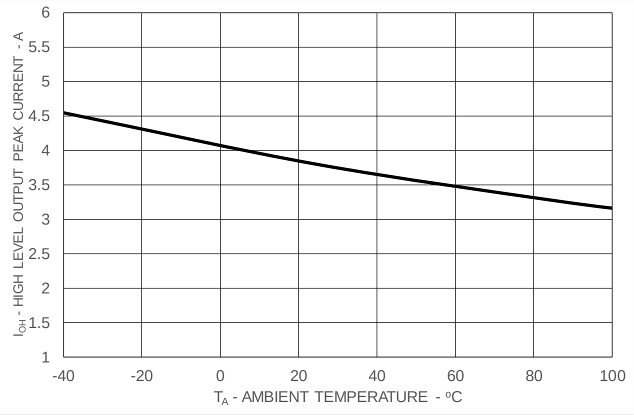


Figure 1. I_{OH} vs. temperature

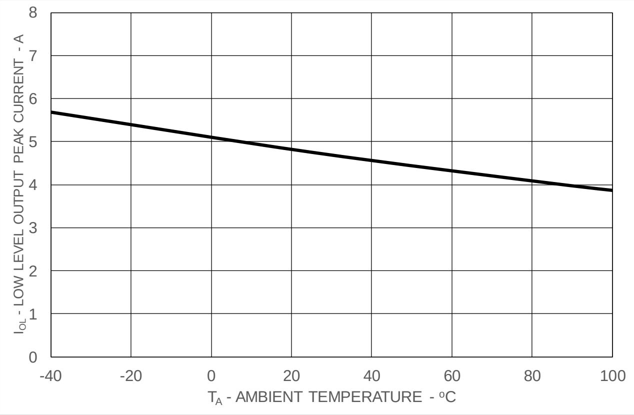


Figure 2. I_{OL} vs. Temperature

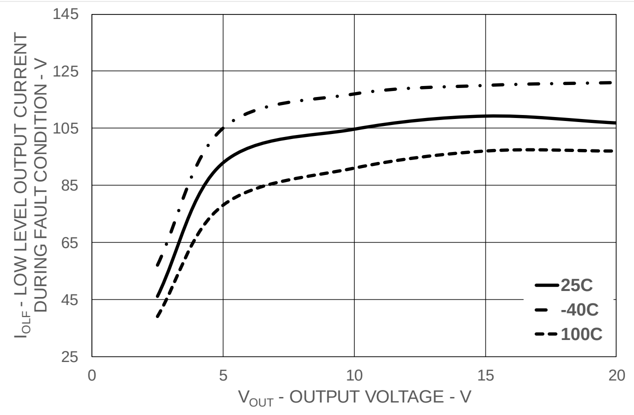


Figure 3. I_{OLF} vs. V_{OUT}

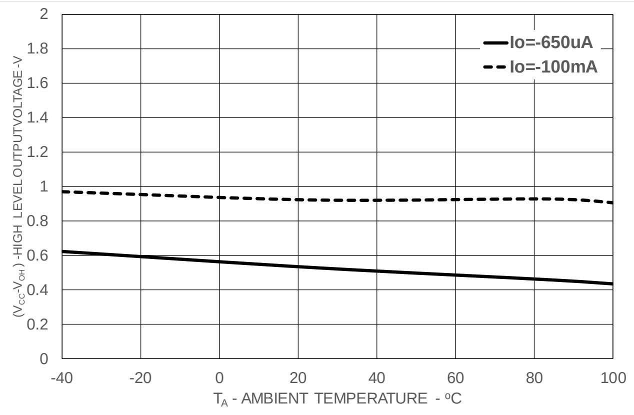


Figure 4. V_{OH} vs. Temperature

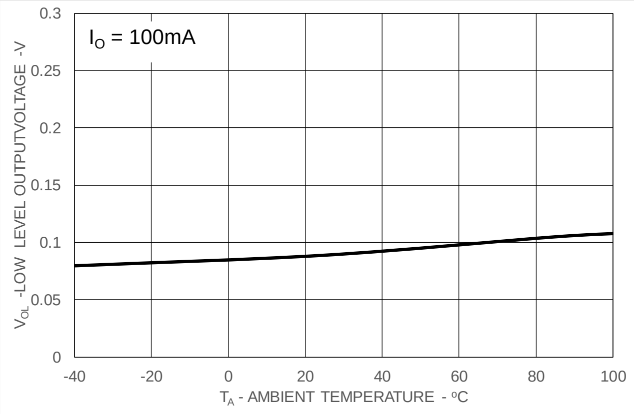


Figure 5. V_{OL} vs. Temperature

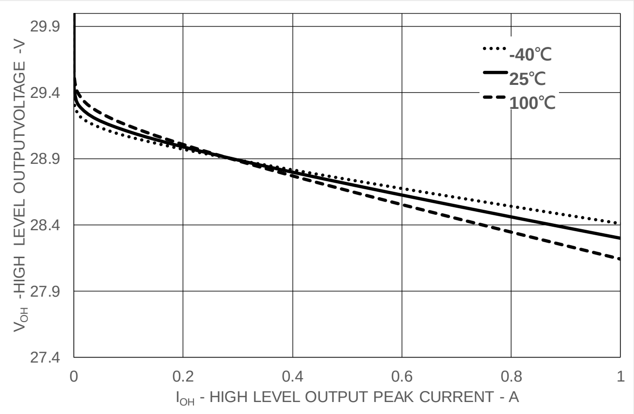


Figure 6. V_{OH} vs. I_{OH}

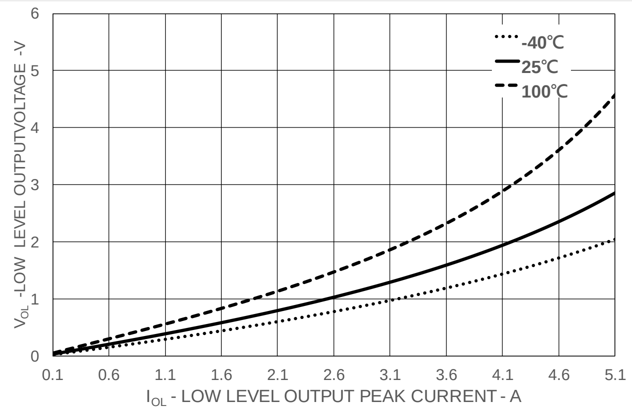


Figure 7. V_{OL} vs. I_{OL}

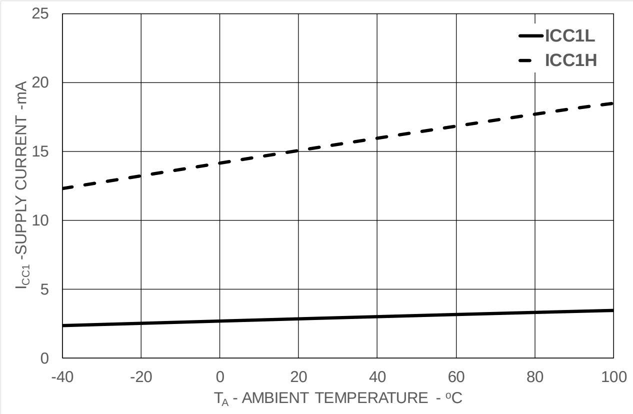


Figure 8. I_{CC1} vs. Temperature

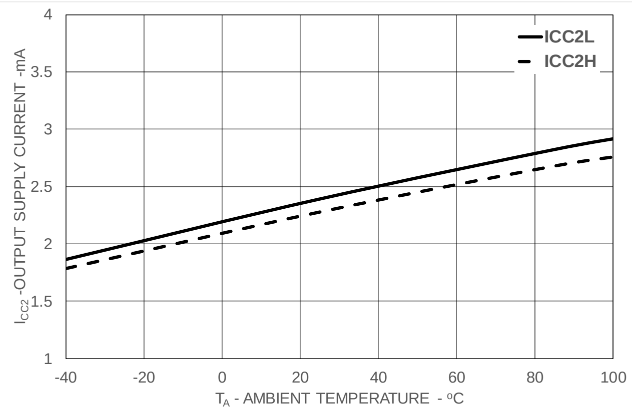


Figure 9. I_{CC2} vs. Temperature

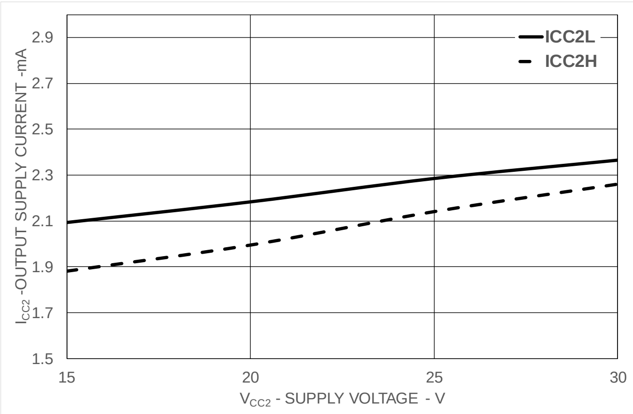


Figure 10. I_{CC2} vs. V_{CC2}

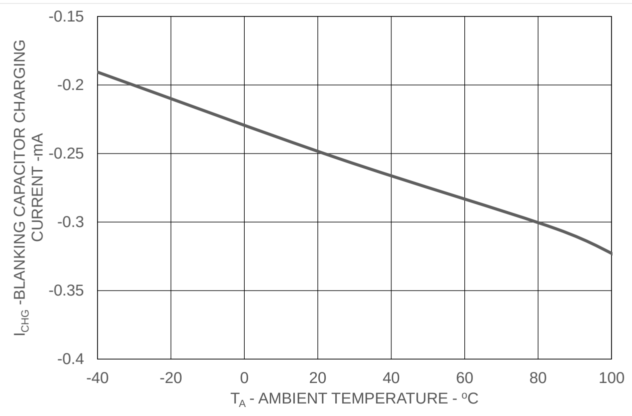


Figure 11. I_{CHG} vs. Temperature

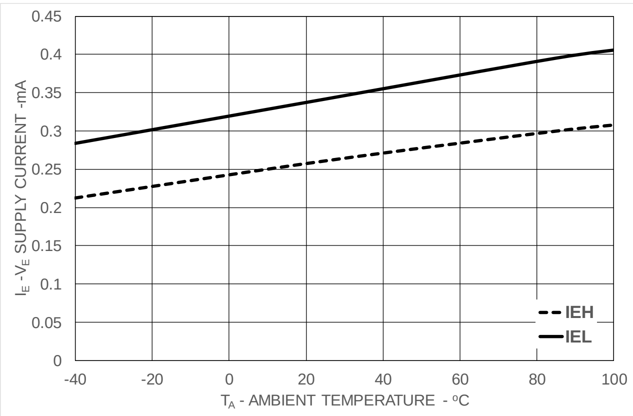
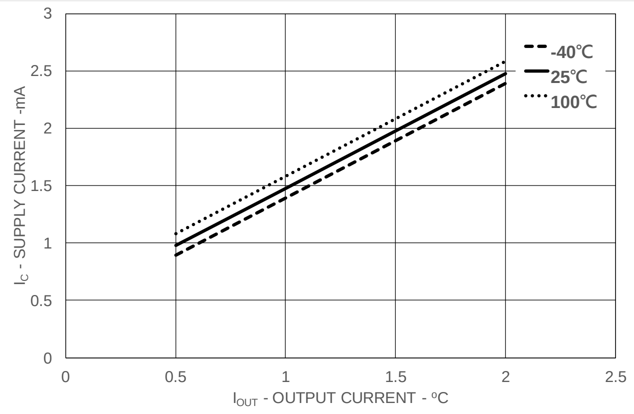


Figure 12. I_E vs. Temperature



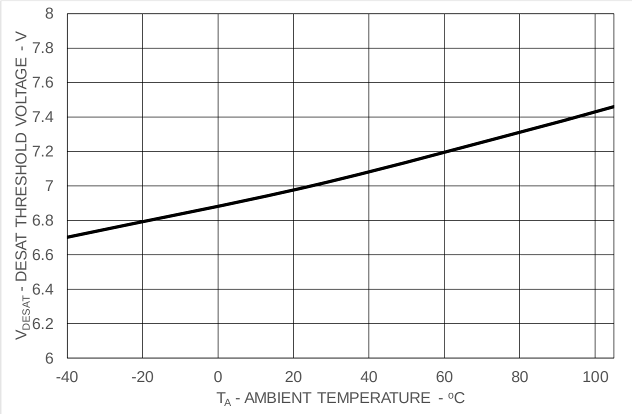
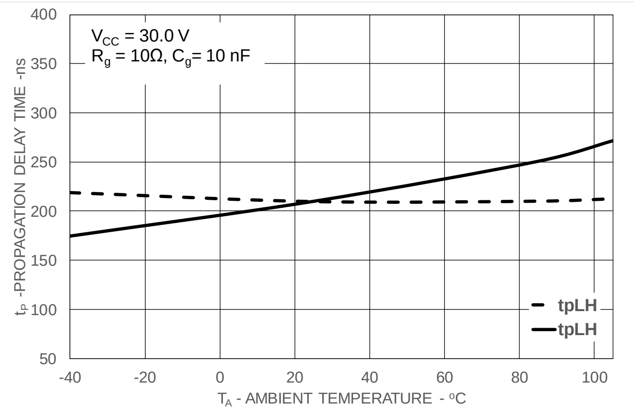


Figure 13. I_C vs. I_{OUT}

Figure 14. DESAT Threshold vs. Temperature



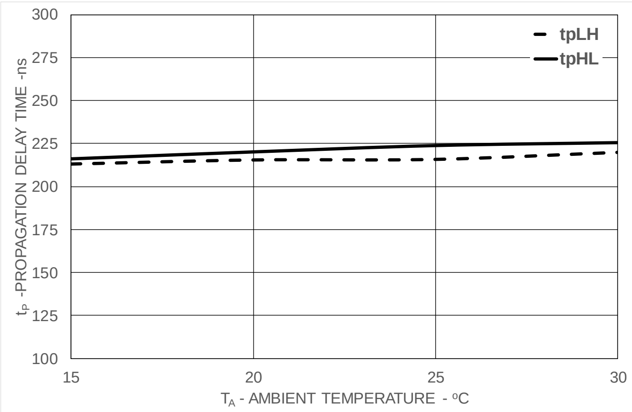
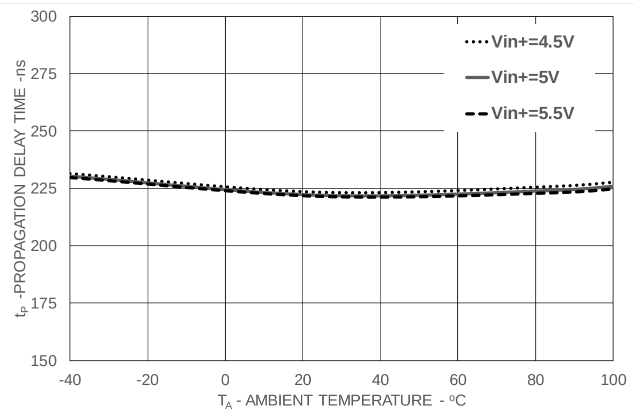


Figure 15. Propagation Delay vs. Temperature

Figure 16. Propagation Delay vs. Supply Voltage



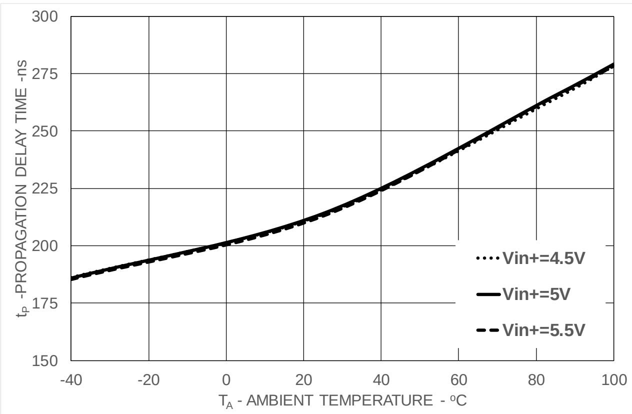
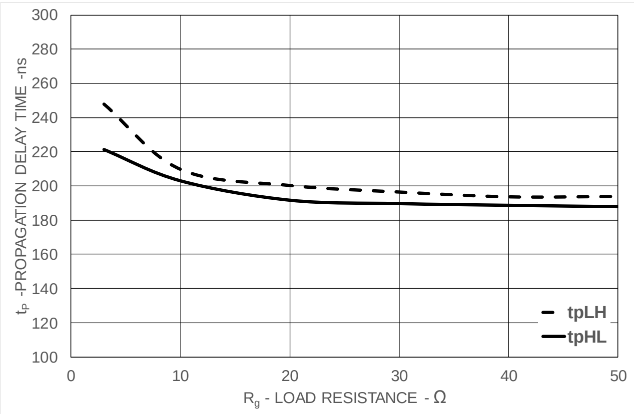


Figure 17. Vin to high Propagation Delay vs. Ta

Figure 18. Vin to Low Propagation Delay vs. Ta



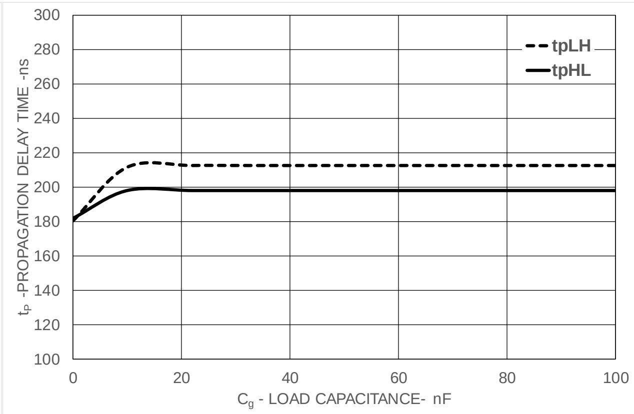
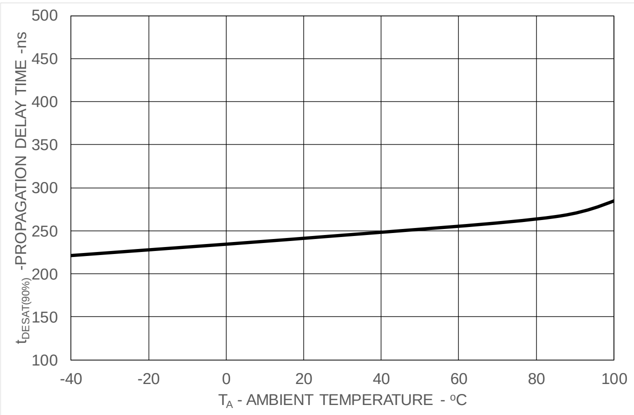


Figure 19. Propagation Delay vs. Rg

Figure 20. Propagation Delay vs. Cg



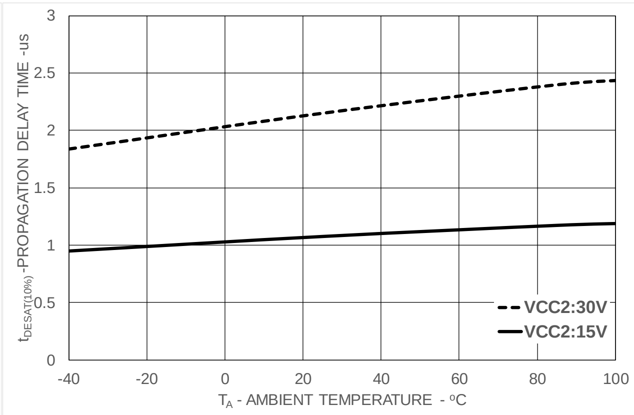
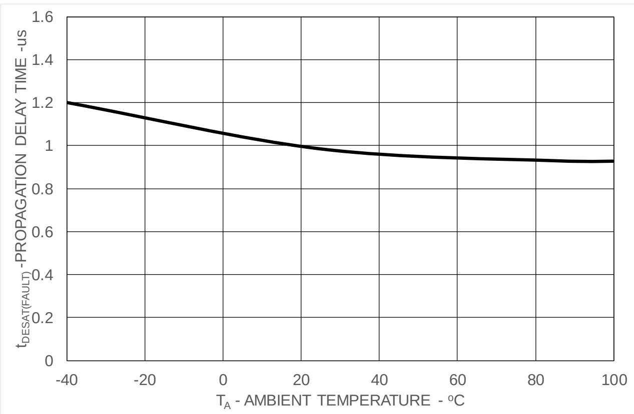


Figure 21. DESAT sense to 90% V_{OUT} delay vs. T_A

Figure 22. DESAT sense to 10% V_{OUT} delay vs. T_A



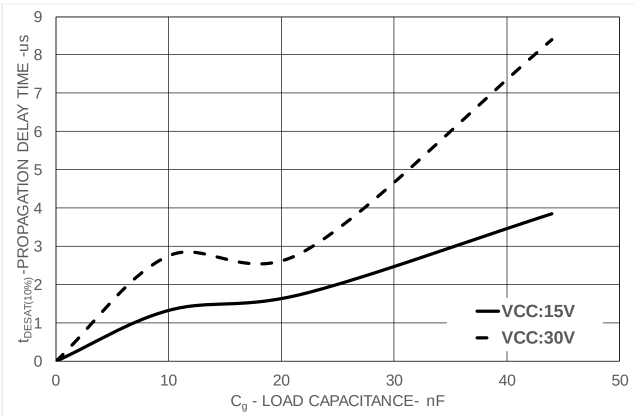


Figure 23. DESAT sense to low level fault signal delay vs. T_A

Figure 24. DESAT sense to 10% V_{OUT} delay vs. Cg

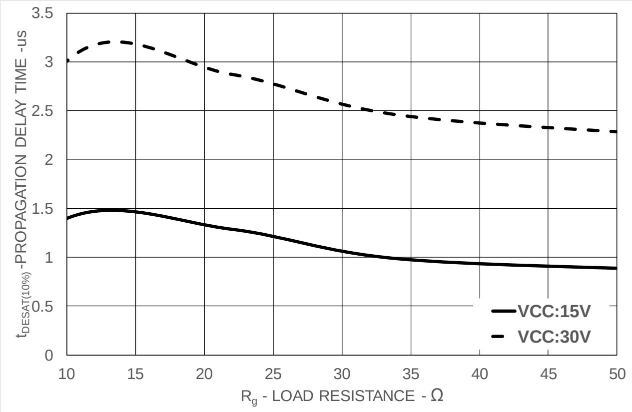


Figure 25. DESAT sense to 10% V_{OUT} delay vs. Rg

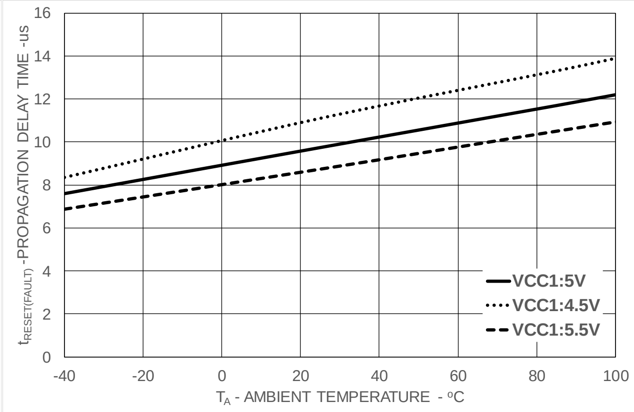


Figure 26. RESET to high level fault signal delay vs. Rg

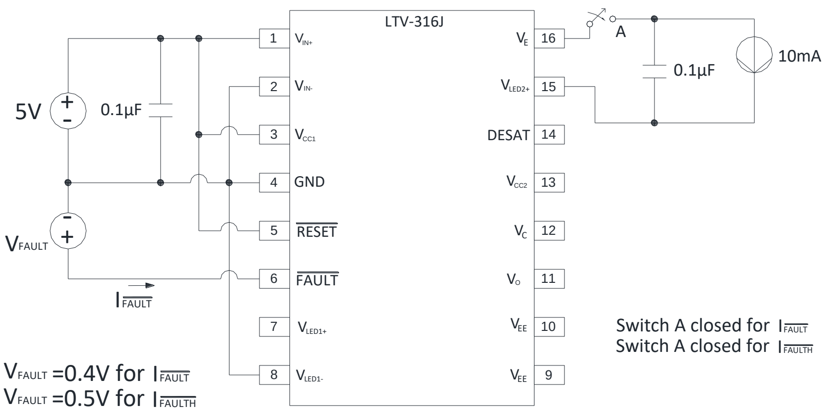


Figure 27. Fault Output Current($I_{\overline{FAULTL}}$) and($I_{\overline{FAULTH}}$) Test Circuit

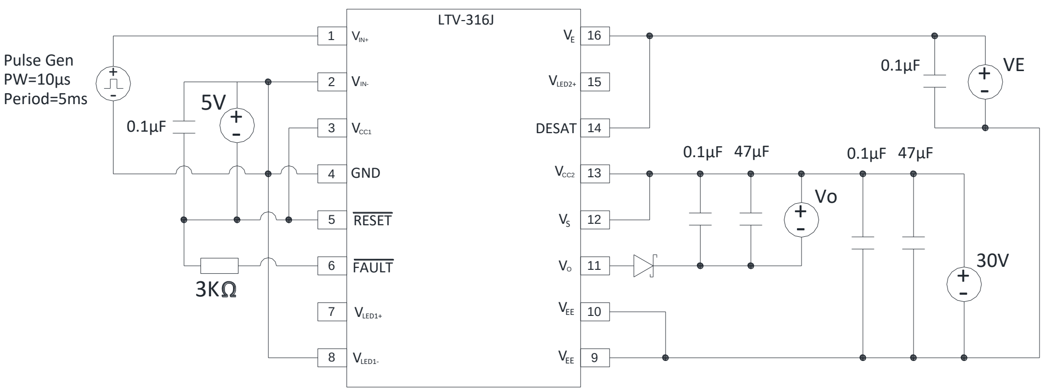


Figure 28. High Level Output Current(I_{OH}) Test Circuit

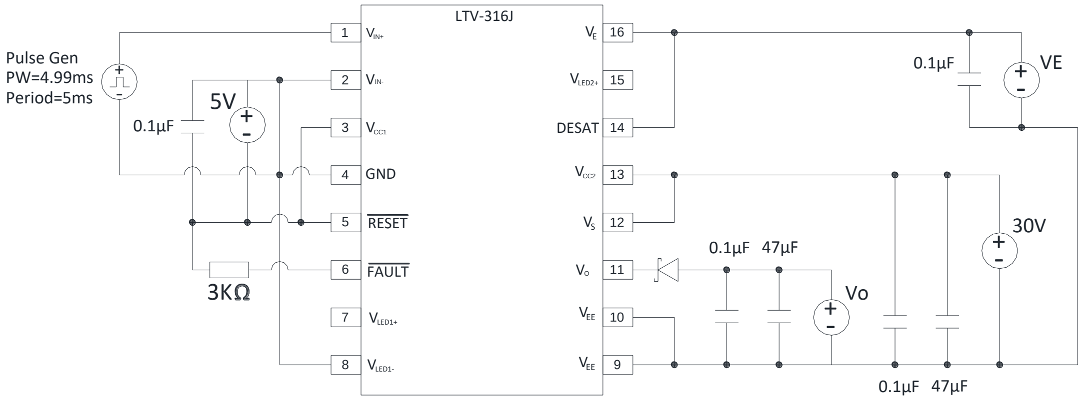


Figure 29. Low Level Output Current(I_{OL}) Test Circuit

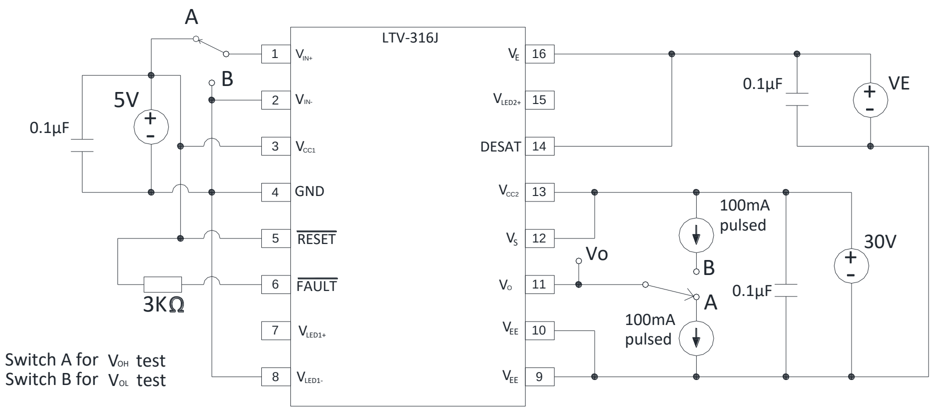


Figure 30. High Level (V_{OH}) and (V_{OL}) Output Voltage Test Circuit

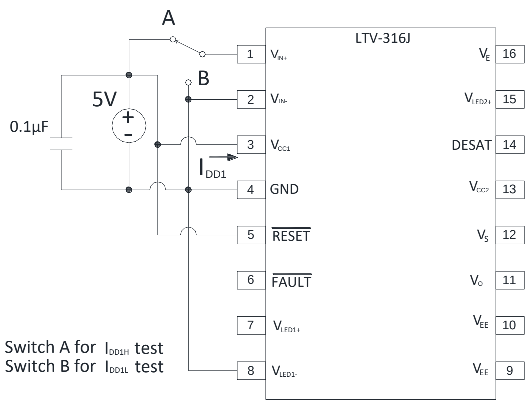


Figure 31. High Level (I_{CC1H}) and Low Level (I_{CC1L}) Supply Current Test Circuit

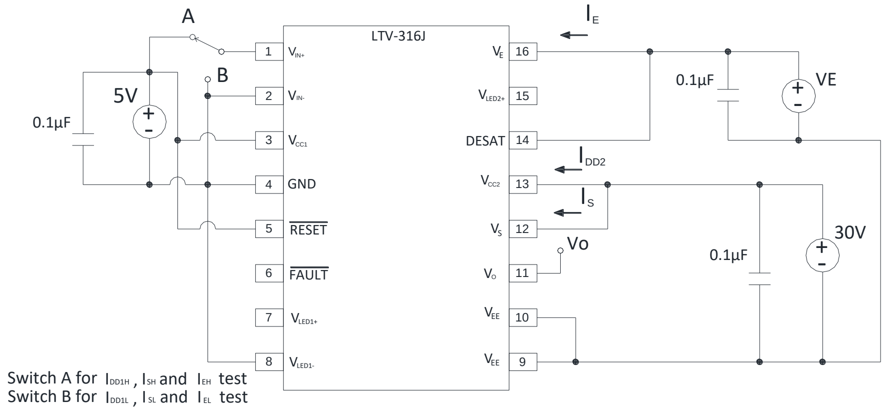


Figure 32. High Level (I_{CC2H}) and Low Level (I_{CC2L}) Supply Current,

High Level (I_{SH}) and Low Level (I_{SL}) Sourse Current

VE High Level (IEH) and VE Low Level (IEL) Supply Current Test Circuit

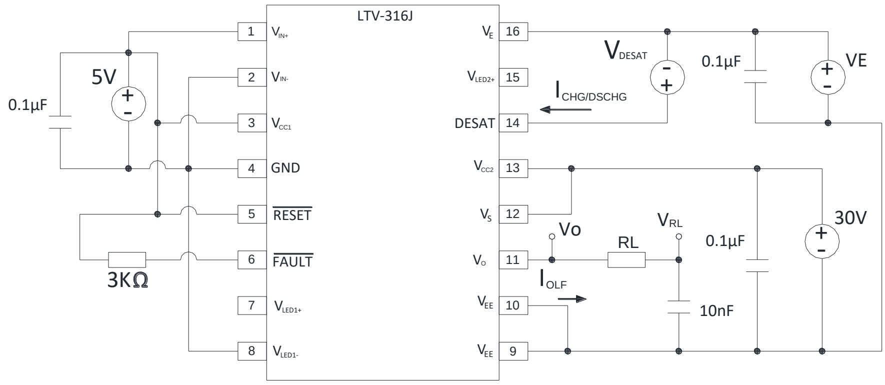


Figure 33. Low Level Output Current During Fault Condition(I_{OLF}) and Blanking Capacitor Charge Current(I_{CHG}),

Blanking Capacitor Discharge Current(I_{DSCHG}) and DESAT Threshold(V_{DESAT}) Test Circuit

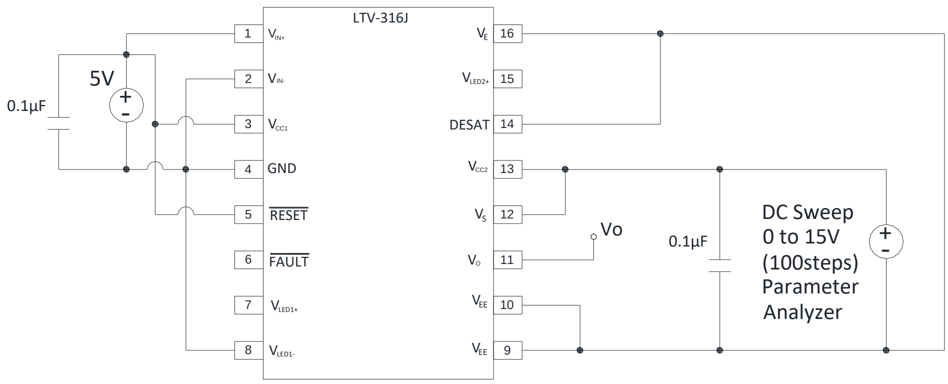


Figure 34. Under Voltage Lockout Threshold(V_{UVLO+})and (V_{UVLO-})Test Circuit

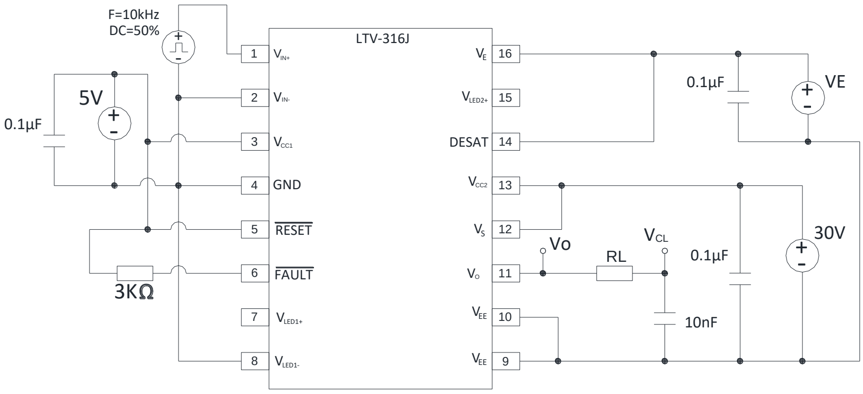


Figure 35. Propagation Delay(t_{PLH}, t_{PHL}),Pulse Width Distortion (PWD), Rising Time(tr) and Falling time(tf) Test Circuit

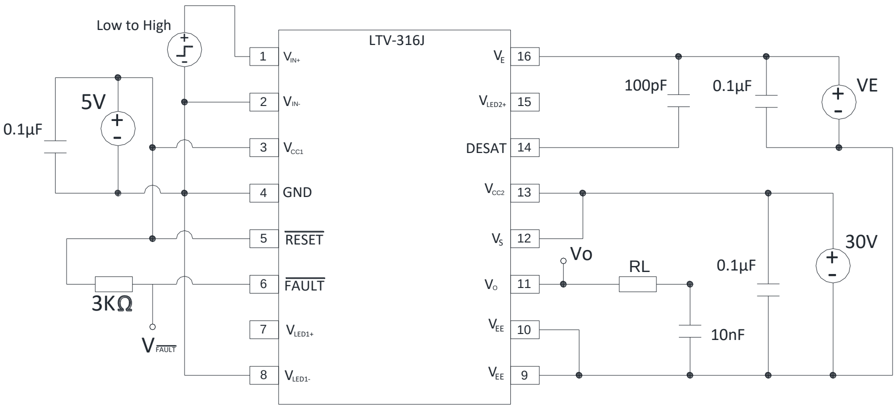


Figure 36.DESAT Sense ($t_{DESAT(90\%)}$, $t_{DESAT(10\%)}$), DESAT Fault($t_{DESAT(\overline{FAULT})}$, $t_{DESAT(LOW)}$) Test Circuit

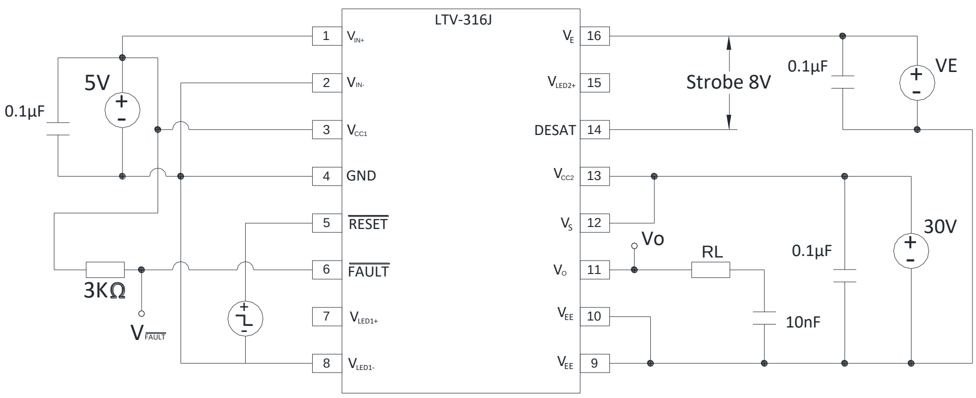


Figure 37. Reset Delay ($t_{\overline{RESET}(\overline{FAULT})}$) Test Circuit

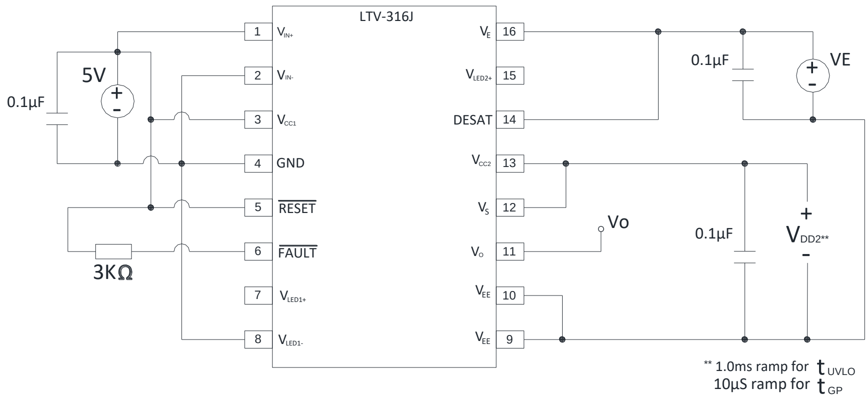


Figure 38. Under Voltage Lockout Delay(tUVLO) Test Circuit

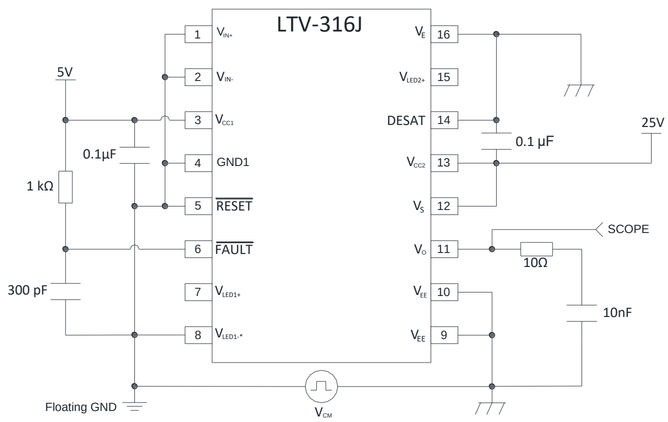


Figure 39. Common Mode Low (CML) Test Circuit LED1 OFF

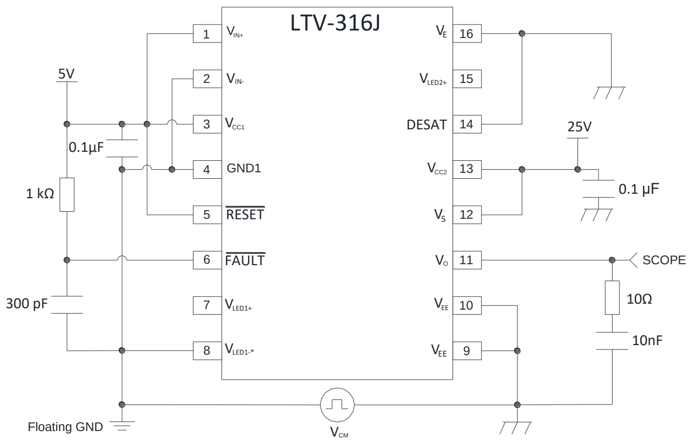


Figure 40. Common Mode Low (CMH) Test Circuit LED1 ON

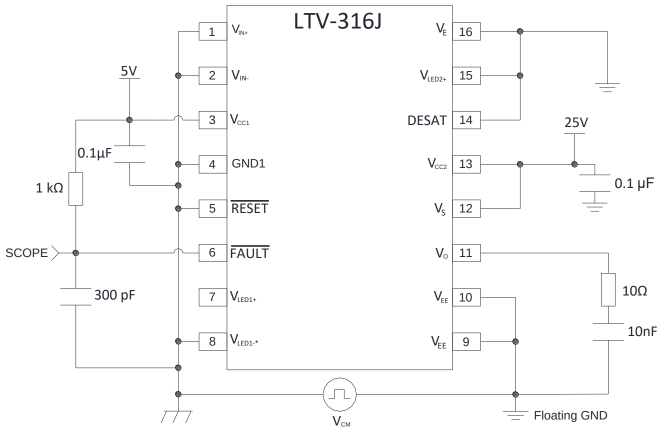


Figure 41. Common Mode Low (CMH) Test Circuit LED2 OFF

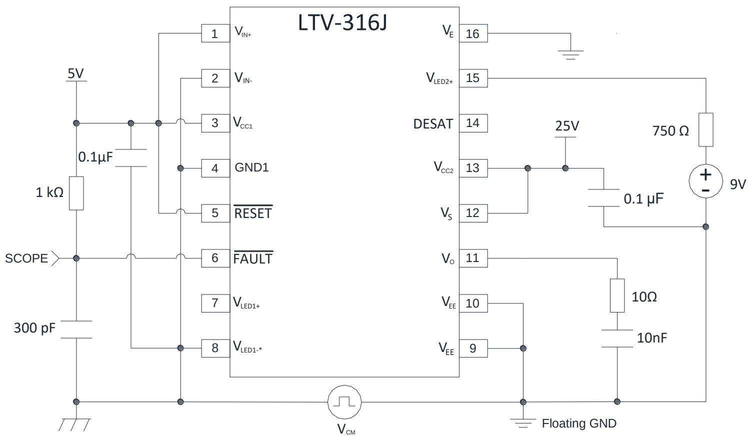


Figure 42. Common Mode Low (CML) Test Circuit LED2 ON

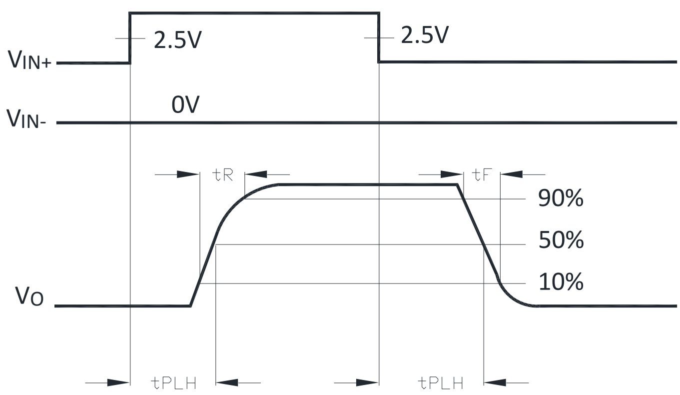


Figure 43. Propagation Delay(tPLH, tPHL), Rising Time(tr), Falling Time(tf) Waveforms Diagram

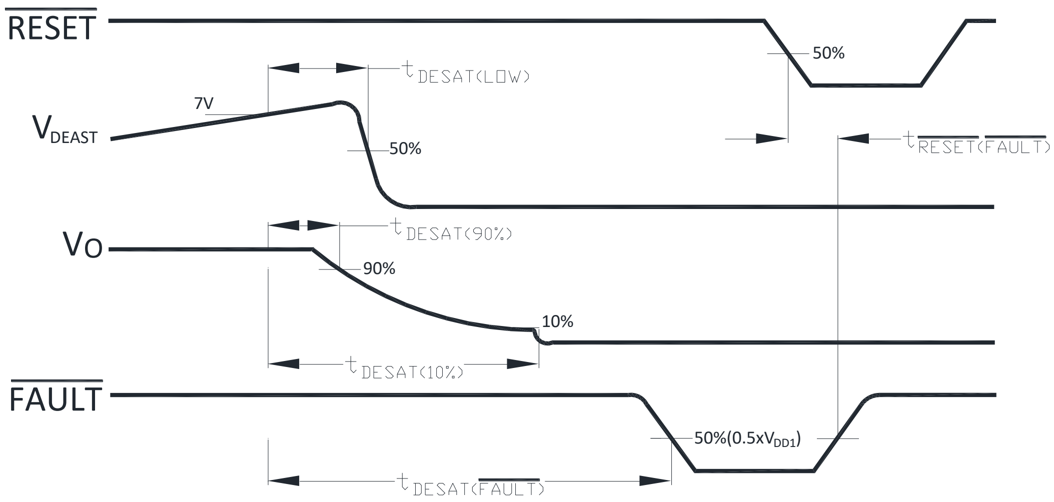


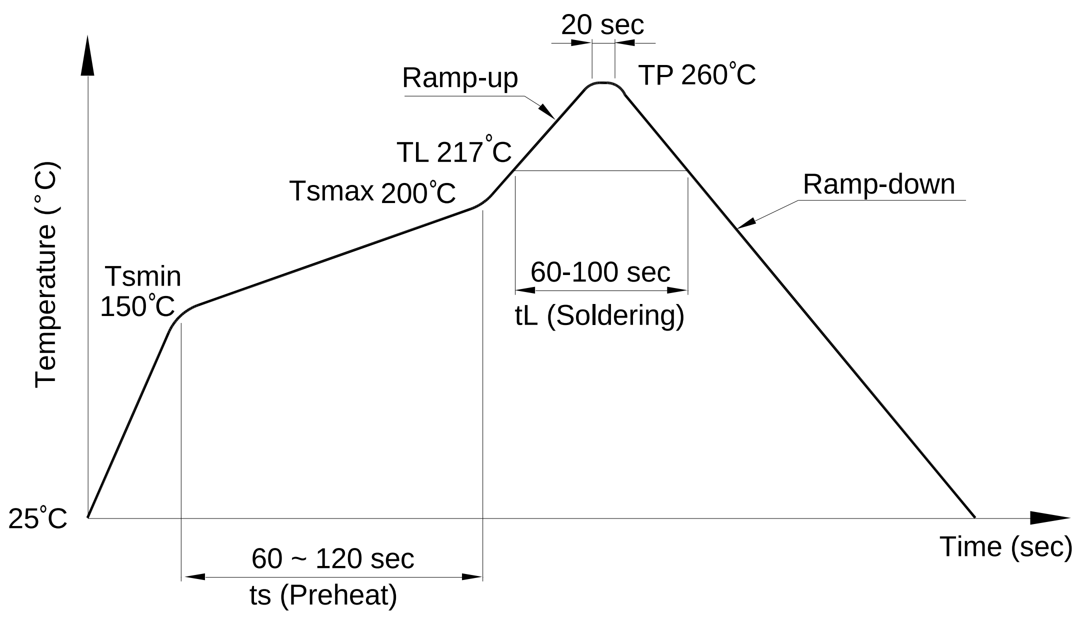
Figure 44. Definitions for Fault Reset Input (RESET), Desaturation Voltage Input (DESAT), Output Voltage (VO) and Fault Output (FAULT) Timing Waveforms Diagram

8. TEMPERATURE PROFILE OF SOLDERING

8.1 IR Reflow soldering (JEDEC-STD-020C compliant)

One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

Profile item	Conditions
Preheat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (min to max) (ts)	 150˚C 200˚C 90±30 sec
Soldering zone - Temperature (T_L) - Time (t_L)	 217˚C 60 ~ 100 sec
Peak Temperature (T_P)	260˚C
Ramp-up rate	3˚C / sec max.
Ramp-down rate	3~6˚C / sec



8.2 Wave soldering (JEDEC22A111 compliant)

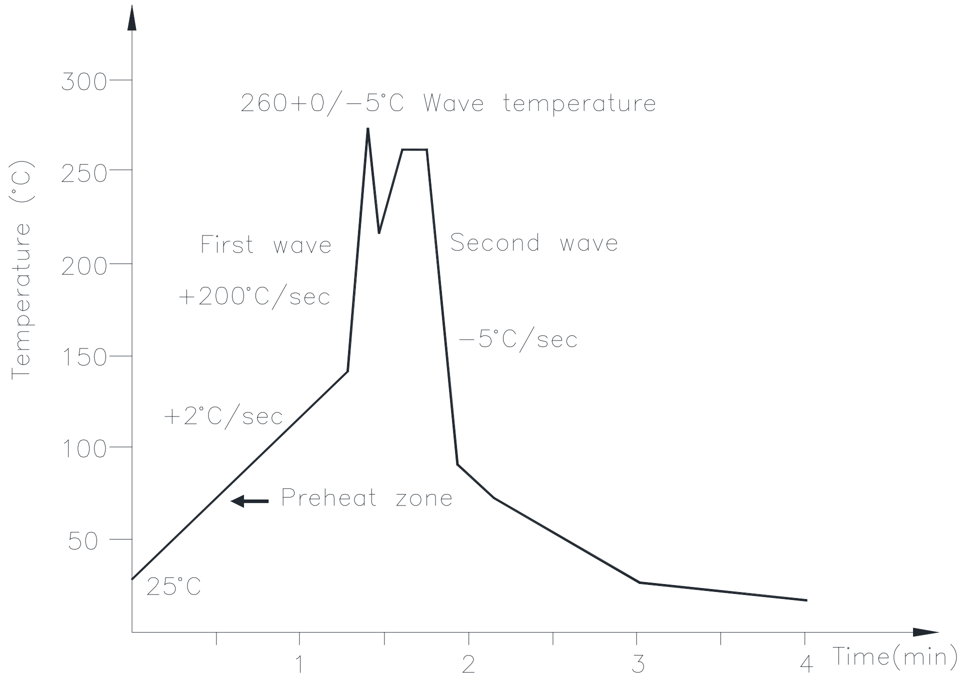
One time soldering is recommended within the condition of temperature.

Temperature: 260+0/-5˚C

Time: 10 sec.

Preheat temperature:25 to 140˚C

Preheat time: 30 to 80 sec.



8.3 Hand soldering by soldering iron

Allow single lead soldering in every single process. One time soldering is recommended.

Temperature: 380+0/-5˚C

Time: 3 sec max.

9. Notes:

Specifications of the products displayed herein are subject to change without notice.

The products shown in this publication are designed for the general use in electronic applications such as office automation equipment, communications devices, audio/visual equipment, electrical instrumentation and application. For equipment/devices where high reliability or safety is required, such as space applications, nuclear power control equipment, medical equipment, etc, please contact our sales representatives.