



# **CD4052H**

## **Dual 4-channel Analog Multiplexer/Demultiplexer**

### **Product Specification**

**Specification Revision History:**

<b>Version</b>	<b>Date</b>	<b>Description</b>
2022-04-A1	2022-04	New



# Contents

<b>1、 General Description.....</b>	<b>1</b>
<b>2、 Block Diagram And Pin Description .....</b>	<b>3</b>
2.1、 Block Diagram .....	3
2.2、 Pin Configurations.....	5
2.3、 Pin Description .....	6
2.4、 Function Table.....	6
<b>3、 Electrical Parameter .....</b>	<b>7</b>
3.1、 Absolute Maximum Ratings.....	7
3.2、 Recommended Operating Conditions .....	7
3.3、 Electrical Characteristics .....	8
3.3.1、 DC Characteristics 1 .....	8
3.3.2、 DC Characteristics 2 .....	9
3.3.3、 AC Characteristics 1 .....	9
3.3.4、 AC Characteristics 2 .....	10
<b>4、 Testing Circuit .....</b>	<b>10</b>
4.1、 DC Testing Circuit .....	10
4.2、 ON resistance Testing Circuit .....	11
4.3、 ON resistance Waveforms.....	11
4.4、 AC Testing Circuit 1 .....	12
4.5、 AC Testing Waveforms.....	12
4.6、 AC Testing Circuit 2 .....	13
4.7、 Measurement Points .....	15
4.8、 Test Data .....	15
<b>5、 Package Information .....</b>	<b>16</b>
5.1、 DIP16 .....	16
5.2、 SOP16 .....	17
5.3、 TSSOP16.....	18
<b>6、 Statements And Notes .....</b>	<b>19</b>
6.1、 The name and content of Hazardous substances or Elements in the product.....	19
6.2、 Notion.....	19



## 1、 General Description

The CD4052H is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logic includes two select inputs (S1 and S2) and an active LOW enable input ( $\bar{E}$ ). Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY0 to nY3) and the other side connected to a common input/output (nZ). With  $\bar{E}$  LOW, one of the four switches is selected (low-impedance ON-state) by S1 and S2. With  $\bar{E}$  HIGH, all switches are in the high-impedance OFF-state, independent of S1 and S2. If break before make is needed, then it is necessary to use the enable input.

$V_{DD}$  and  $V_{SS}$  are the supply voltage connections for the digital control inputs (S1 and S2, and  $\bar{E}$ ). The  $V_{DD}$  to  $V_{SS}$  range is 3V to 18V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between  $V_{DD}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{DD}-V_{EE}$  may not exceed 18V. Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input. For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to  $V_{SS}$  (typically ground).  $V_{EE}$  and  $V_{SS}$  are the supply voltage connections for the switches.

### Features:

- Wide supply voltage range from 3V to 18V
- Fully static operation
- 5V, 10V and 18V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +105°C
- Packaging information: DIP16/SOP16/TSSOP16

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4052HDA16.TB	DIP16	CD4052H	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4052HSA16.TB	SOP16(1)	CD4052H	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4052HSA16.TB	SOP16(2)	CD4052H	50 PCS/tube	100 tube/box	5000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4052HTA16.TB	TSSOP16	CD4052H	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

**Reel packing specifications:**

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4052HSA16.TR	SOP16	CD4052H	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4052HTA16.TR	TSSOP16	CD4052H	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

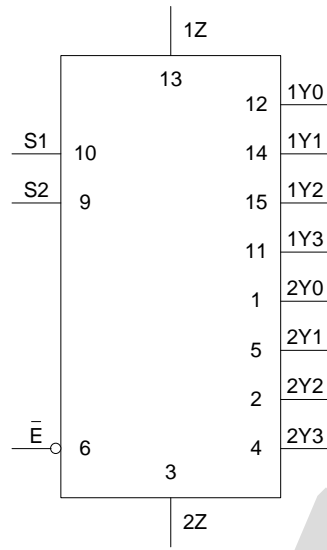


Figure 1. Logic symbol

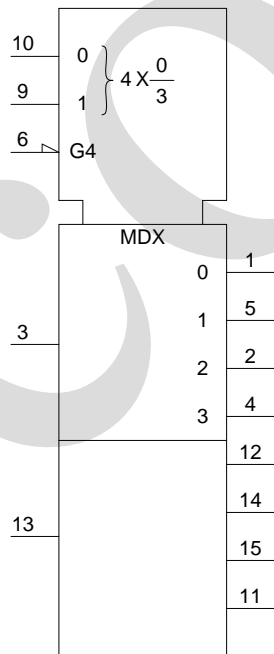


Figure 2. IEC logic symbol

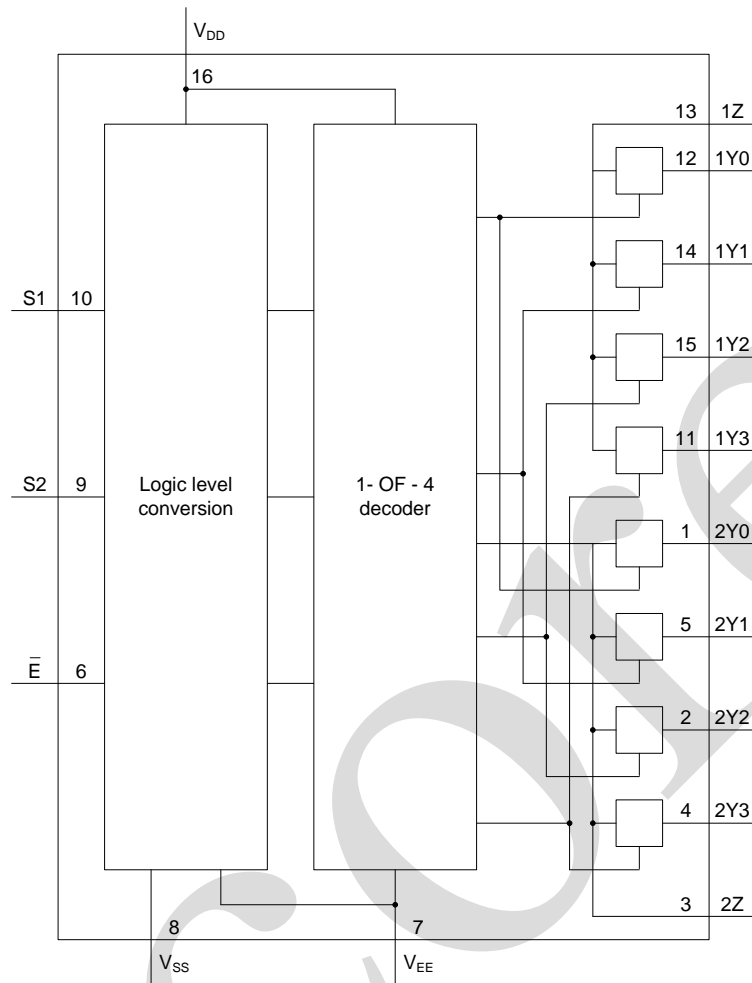


Figure 3. Functional diagram

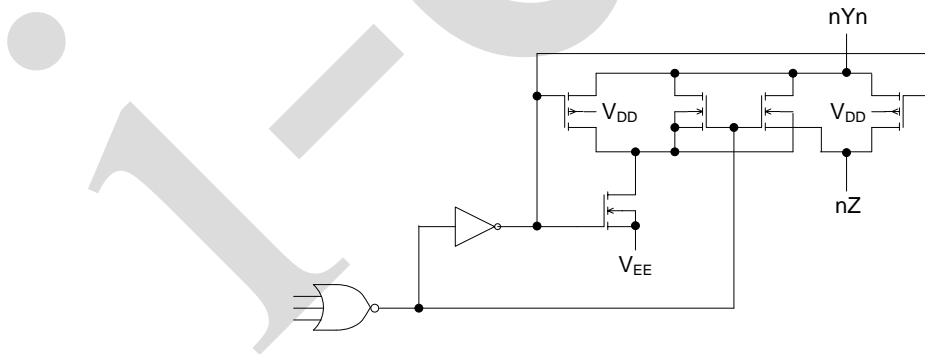


Figure 4. Schematic diagram (one switch)

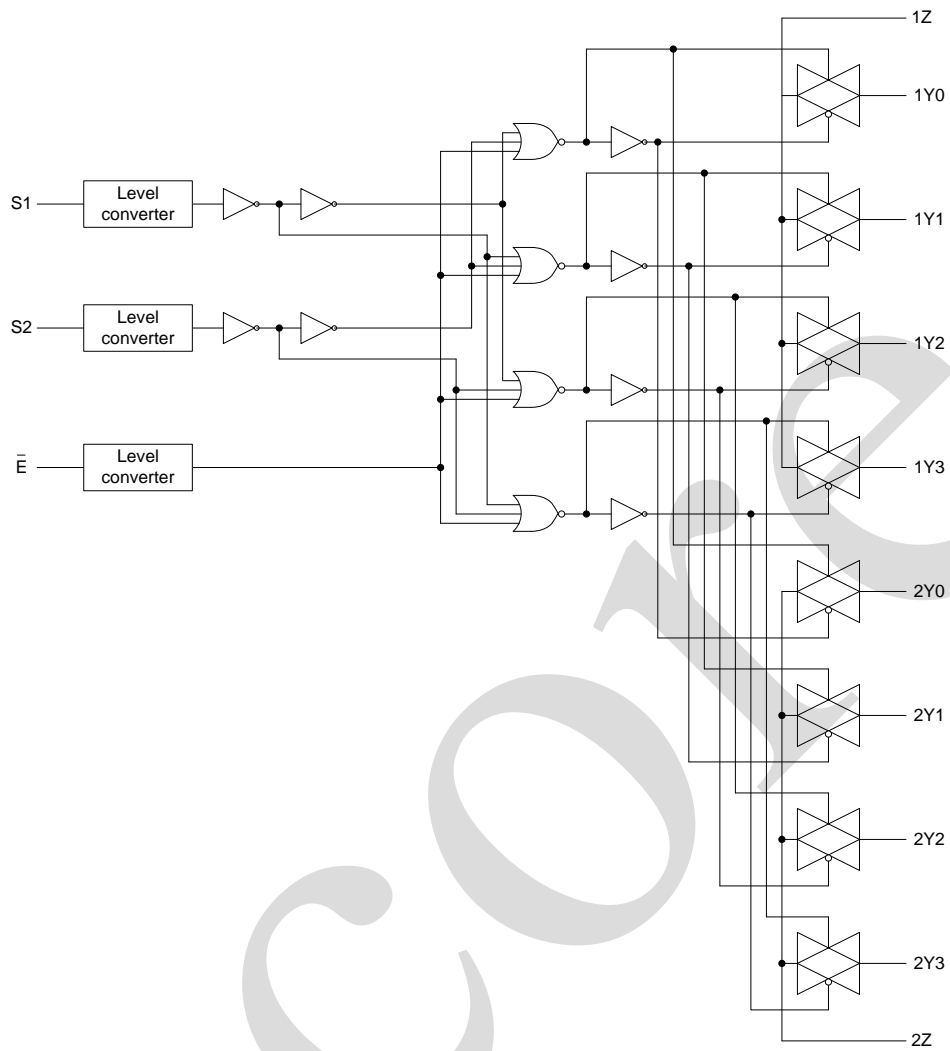
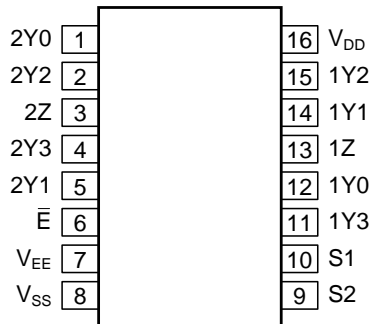


Figure 5. Logic diagram

## 2.2. Pin Configurations





## 2.3、Pin Description

Pin No.	Pin Name	Description
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common output or input
4	2Y3	independent input or output
5	2Y1	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V <sub>EE</sub>	supply voltage
8	V <sub>SS</sub>	ground (0V)
9	S2	select input
10	S1	select input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common output or input
14	1Y1	independent input or output
15	1Y2	independent input or output
16	V <sub>DD</sub>	supply voltage

## 2.4、Function Table

Input			Channel ON
$\bar{E}$	S2	S1	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.





## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

( $T_{amb}=25^{\circ}\text{C}$ , voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	$V_{DD}$	-	-0.5	+21	V
supply voltage	$V_{EE}$	referenced to $V_{DD}$	-21	+0.5	V
input voltage	$V_I$	-	-0.5	$V_{DD}+0.5$	V
input clamping current	$I_{IK}$	$V_I < -0.5\text{V}$ or $V_I > V_{DD}+0.5\text{V}$	-	$\pm 10$	mA
Input/output current	$I_{IO}$	-	-	$\pm 10$	mA
supply current	$I_{DD}$	-	-	50	mA
storage temperature	$T_{stg}$	-	-65	+150	$^{\circ}\text{C}$
ambient temperature	$T_{amb}$	-	-40	+105	$^{\circ}\text{C}$
total power dissipation	$P_{tot}$	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	$T_L$	10s	DIP	245	$^{\circ}\text{C}$
			SOP	250	$^{\circ}\text{C}$

Note:

[1] For DIP16 packages: above  $70^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 12mW/K.

[2] For SOP16 packages: above  $70^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above  $60^{\circ}\text{C}$  the value of  $P_{tot}$  derates linearly with 5.5mW/K.

### 3.2、Recommended Operating Conditions

( $T_{amb}=25^{\circ}\text{C}$ ;  $R_L=10\text{k}\Omega$ ;  $C_L=50\text{pF}$ ;  $\bar{E}=V_{DD}$ ;  $V_{is}=V_{DD}=5\text{V}$ .)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	$V_{DD}$	-	3	-	18	V
supply voltage	$V_{EE}$	-	-15	-	0	V
supply voltage	$V_{DD}-V_{EE}$	-	3	-	18	V
input voltage	$V_I$	-	0	-	$V_{DD}$	V
ambient temperature	$T_{amb}$	in free air	-40	-	+105	$^{\circ}\text{C}$
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{DD}=5\text{V}$	-	-	3.75	us/V
		$V_{DD}=10\text{V}$	-	-	0.5	us/V
		$V_{DD}=18\text{V}$	-	-	0.08	us/V



### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

( $T_{amb}=25^{\circ}\text{C}$ ,  $V_{SS}=V_{EE}=0\text{V}$ ;  $V_I=V_{SS}$  or  $V_{DD}$ ,  $I_{SW}=200\mu\text{A}$ , unless otherwise specified.)

Parameter	Symbol	Conditions (V)	$T_{amb}=25^{\circ}\text{C}$			Unit	
			Min.	Typ.	Max.		
HIGH-level input voltage	$V_{IH}$	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	3.5	-	-	V
			$V_{DD}=10\text{V}$	7.0	-	-	V
			$V_{DD}=18\text{V}$	12.6	-	-	V
LOW-level input voltage	$V_{IL}$	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	-	-	1.5	V
			$V_{DD}=10\text{V}$	-	-	3.0	V
			$V_{DD}=18\text{V}$	-	-	5.4	V
supply current	$I_{DD}$	$I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	-	5	$\mu\text{A}$
			$V_{DD}=10\text{V}$	-	-	10	$\mu\text{A}$
			$V_{DD}=18\text{V}$	-	-	20	$\mu\text{A}$
input leakage current	$I_I$	$V_{DD}=18\text{V}$	-	-	$\pm 0.1$	$\mu\text{A}$	
OFF-state leakage current	$I_{S(OFF)}$	$V_{DD}=18\text{V}$	Z port; all channels OFF; see Figure 6	-	-	1000	nA
			Y port; per channel; see Figure 7	-	-	200	nA
ON resistance (peak)	$R_{ON(peak)}$	$V_I=0\text{V}$ to $V_{DD}-V_{EE}$ ; see Figure 8 and Figure 9	$V_{DD}-V_{EE}=5\text{V}$	-	117	836	$\Omega$
			$V_{DD}-V_{EE}=10\text{V}$	-	58	178	$\Omega$
			$V_{DD}-V_{EE}=15\text{V}$	-	41	120	$\Omega$
			$V_{DD}-V_{EE}=20\text{V}$	-	36	105	$\Omega$
ON resistance (rail)	$R_{ON(rail)}$	$V_I=0\text{V}$ ; see Figure 8 and Figure 9	$V_{DD}-V_{EE}=5\text{V}$	-	44	130	$\Omega$
			$V_{DD}-V_{EE}=10\text{V}$	-	29	93	$\Omega$
			$V_{DD}-V_{EE}=15\text{V}$	-	24	69	$\Omega$
			$V_{DD}-V_{EE}=20\text{V}$	-	22	63	$\Omega$
		$V_I=V_{DD}-V_{EE}$ ; see Figure 8 and Figure 9	$V_{DD}-V_{EE}=5\text{V}$	-	82	249	$\Omega$
			$V_{DD}-V_{EE}=10\text{V}$	-	51	157	$\Omega$
			$V_{DD}-V_{EE}=15\text{V}$	-	41	127	$\Omega$
			$V_{DD}-V_{EE}=20\text{V}$	-	36	112	$\Omega$
ON resistance mismatch between channels	$\Delta R_{ON}$	$V_I=0\text{V}$ to $V_{DD}-V_{EE}$ ; see Figure 8	$V_{DD}-V_{EE}=5\text{V}$	-	25	-	$\Omega$
			$V_{DD}-V_{EE}=10\text{V}$	-	10	-	$\Omega$
			$V_{DD}-V_{EE}=15\text{V}$	-	5	-	$\Omega$
			$V_{DD}-V_{EE}=20\text{V}$	-	5	-	$\Omega$
input capacitance	$C_I$	Sn, $\bar{E}$ inputs	-	-	7.5	pF	



### 3.3.2、DC Characteristics 2

( $T_{amb}=-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{SS}=V_{EE}=0\text{V}$ ;  $V_I=V_{SS}$  or  $V_{DD}$ , unless otherwise specified.)

Parameter	Symbol	Conditions (V)	$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+105^{\circ}\text{C}$		Unit	
			Min.	Min.	Min.	Max.	Min.	Max.		
HIGH-level input voltage	$V_{IH}$	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	3.5	-	3.5	-	3.5	-	V
			$V_{DD}=10\text{V}$	7.0	-	7.0	-	7.0	-	V
			$V_{DD}=18\text{V}$	12.6	-	12.6	-	12.6	-	V
LOW-level input voltage	$V_{IL}$	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	-	1.5	-	1.5	-	1.5	V
			$V_{DD}=10\text{V}$	-	3.0	-	3.0	-	3.0	V
			$V_{DD}=18\text{V}$	-	5.4	-	5.4	-	5.4	V
supply current	$I_{DD}$	$I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	5	-	150	-	150	$\mu\text{A}$
			$V_{DD}=10\text{V}$	-	10	-	300	-	300	$\mu\text{A}$
			$V_{DD}=18\text{V}$	-	20	-	600	-	600	$\mu\text{A}$
input leakage current	$I_I$	$V_{DD}=18\text{V}$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$	

### 3.3.3、AC Characteristics 1

( $T_{amb}=25^{\circ}\text{C}$ ,  $V_{EE}=V_{SS}=0\text{V}$ , unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH to LOW propagation delay time	$t_{PHL}$	nYn, nZ to nZ, nYn; see Figure 11	$V_{DD}=5\text{V}$	-	10	20	ns
			$V_{DD}=10\text{V}$	-	5	10	ns
			$V_{DD}=18\text{V}$	-	5	10	ns
		Sn to nYn, nZ; see Figure 12	$V_{DD}=5\text{V}$	-	150	305	ns
			$V_{DD}=10\text{V}$	-	65	135	ns
			$V_{DD}=18\text{V}$	-	50	100	ns
LOW to HIGH propagation delay	$t_{PLH}$	nYn, nZ to nZ, nYn; see Figure 11	$V_{DD}=5\text{V}$	-	10	20	ns
			$V_{DD}=10\text{V}$	-	5	10	ns
			$V_{DD}=18\text{V}$	-	5	10	ns
		Sn to nYn, nZ; see Figure 12	$V_{DD}=5\text{V}$	-	150	300	ns
			$V_{DD}=10\text{V}$	-	75	150	ns
			$V_{DD}=18\text{V}$	-	50	100	ns
HIGH to OFF-state propagation delay	$t_{PHZ}$	$\bar{E}$ to nYn, nZ; see Figure 13	$V_{DD}=5\text{V}$	-	95	190	ns
			$V_{DD}=10\text{V}$	-	90	180	ns
			$V_{DD}=18\text{V}$	-	85	180	ns
LOW to OFF-state propagation delay	$t_{PLZ}$	$\bar{E}$ to nYn, nZ; see Figure 13	$V_{DD}=5\text{V}$	-	100	205	ns
			$V_{DD}=10\text{V}$	-	90	180	ns
			$V_{DD}=18\text{V}$	-	90	180	ns
OFF-state to HIGH propagation delay	$t_{PZH}$	$\bar{E}$ to nYn, nZ; see Figure 13	$V_{DD}=5\text{V}$	-	130	260	ns
			$V_{DD}=10\text{V}$	-	55	115	ns
			$V_{DD}=18\text{V}$	-	45	85	ns
OFF-state to LOW propagation delay	$t_{PZL}$	$\bar{E}$ to nYn, nZ; see Figure 13	$V_{DD}=5\text{V}$	-	120	240	ns
			$V_{DD}=10\text{V}$	-	50	100	ns
			$V_{DD}=18\text{V}$	-	35	75	ns



## 3.3.4、AC Characteristics 2

( $T_{amb}=25^{\circ}\text{C}$ ,  $V_{EE}=V_{SS}=0\text{V}$ ,  $V_I=0.5V_{DD}$  (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
total harmonic distortion	THD	see Figure 14; $R_L=10\text{k}\Omega$ ; $C_L=15\text{pF}$ ; channel ON; $f_i=1\text{kHz}$	$V_{DD}=5\text{V}$	-	0.25	-	%
			$V_{DD}=10\text{V}$	-	0.04	-	%
			$V_{DD}=18\text{V}$	-	0.04	-	%
-3dB frequency response	$f_{(-3\text{dB})}$	see Figure 15; $R_L=1\text{k}\Omega$ ; $C_L=5\text{pF}$ ; channel ON;	$V_{DD}=5\text{V}$	-	13	-	MHz
			$V_{DD}=10\text{V}$	-	40	-	MHz
			$V_{DD}=18\text{V}$	-	70	-	MHz
isolation (OFF-state)	$\alpha_{iso}$	see Figure 16; $f_i=1\text{MHz}$ ; $R_L=1\text{k}\Omega$ ; $C_L=5\text{pF}$ ; channel OFF; $V_{DD}=10\text{V}$	-	-50	-	dB	
crosstalk voltage	$V_{ct}$	digital inputs to switch; see Figure 17; $R_L=10\text{k}\Omega$ ; $C_L=15\text{pF}$ ; $\bar{E}$ or $\text{Sn}=V_{DD}$ (square-wave); $V_{DD}=10\text{V}$	-	50	-	mV	
crosstalk	Xtalk	between switches; see Figure 18; $f_i=1\text{MHz}$ ; $R_L=1\text{k}\Omega$ ; $V_{DD}=10\text{V}$	-	-50	-	dB	

Note:

[1]  $f_i$  is biased at  $0.5V_{DD}$ ;  $V_I=0.5V_{DD}$  (p-p).

## 4、Testing Circuit

### 4.1、DC Testing Circuit

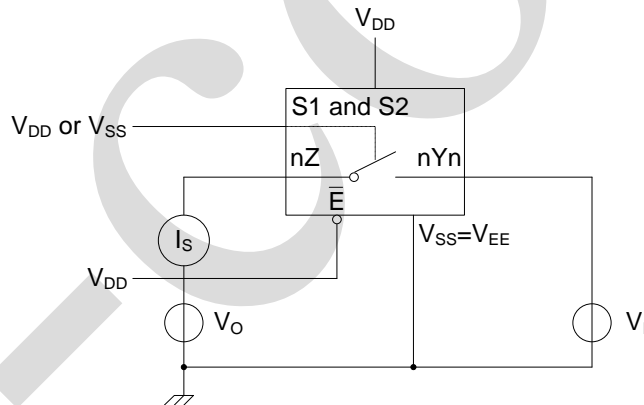


Figure 6. Test circuit for measuring OFF-state leakage current Z port

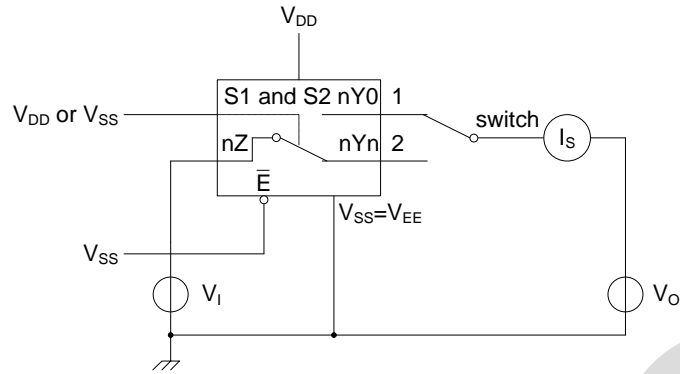


Figure 7. Test circuit for measuring OFF-state leakage current nYn port

## 4.2. ON resistance Testing Circuit

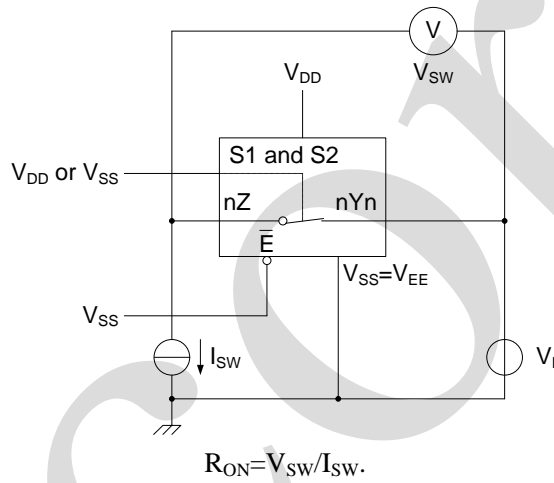


Figure 8. Test circuit for measuring  $R_{ON}$

## 4.3. ON resistance Waveforms

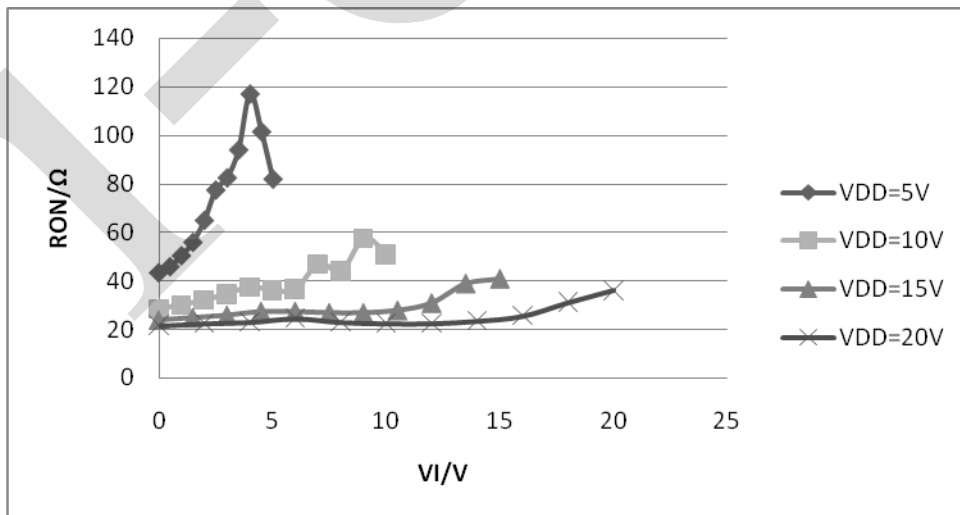


Figure 9. Typical  $R_{ON}$  as a function of input voltage



## 4.4、AC Testing Circuit 1

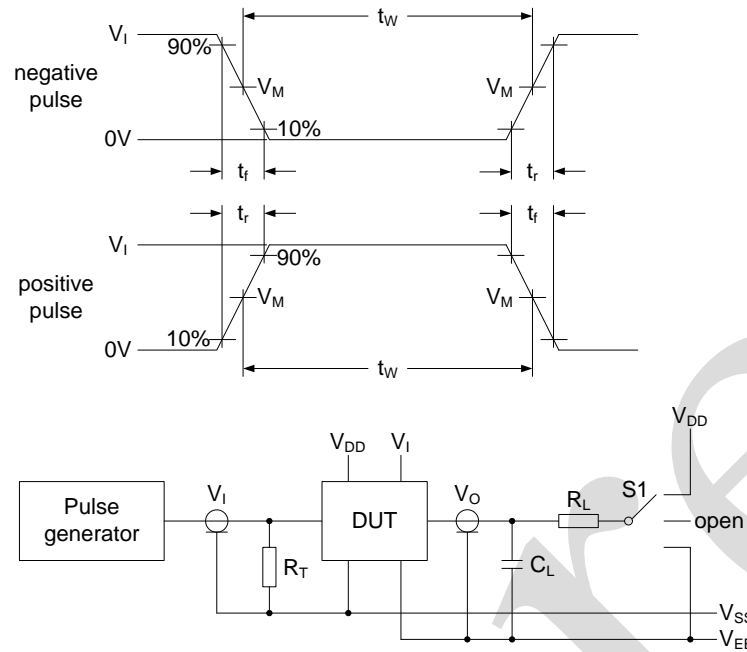


Figure 10. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$R_L$ =Load resistance.

## 4.5、AC Testing Waveforms

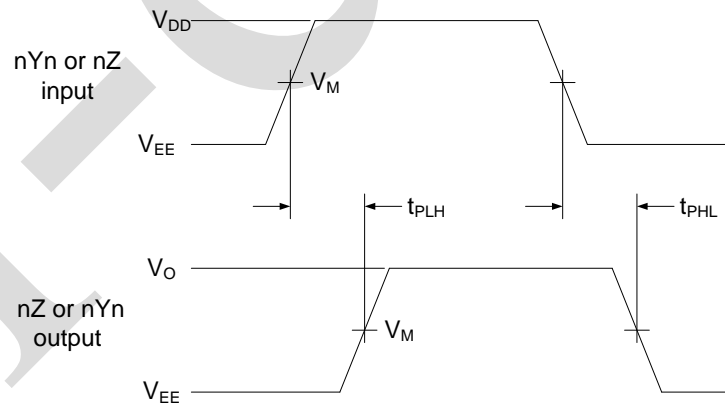


Figure 11. nYn, nZ to nZ, nYn propagation delays

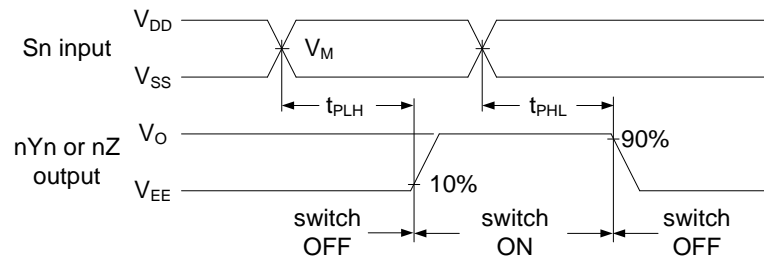


Figure 12. Sn to nYn, nZ propagation delays

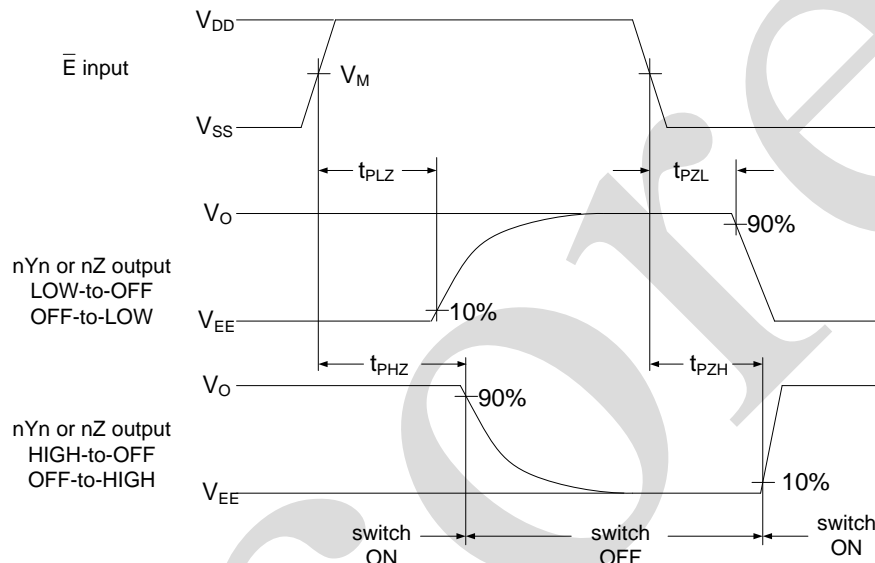


Figure 13. Enable and disable times

## 4.6. AC Testing Circuit 2

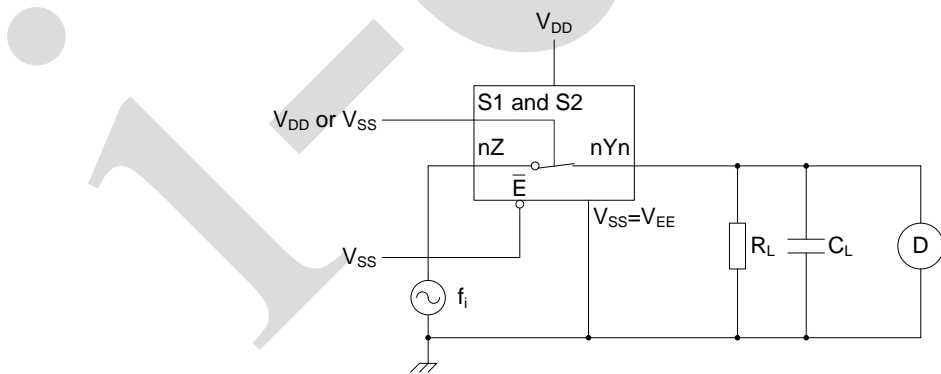


Figure 14. Test circuit for measuring total harmonic distortion

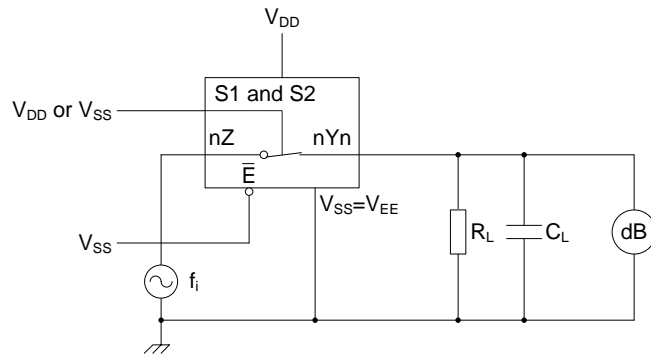


Figure 15. Test circuit for measuring frequency response

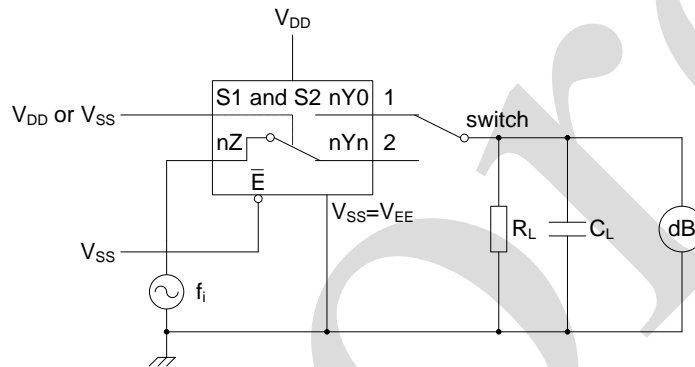
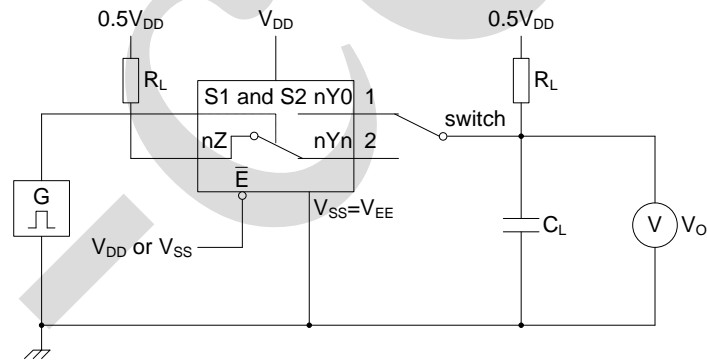
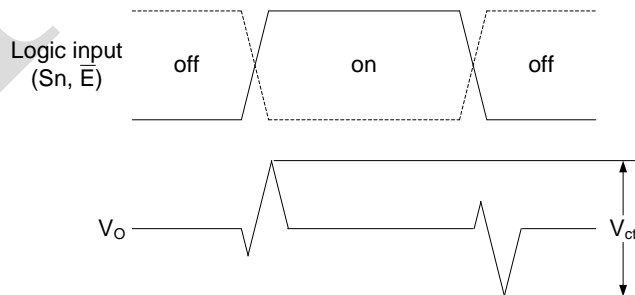


Figure 16. Test circuit for measuring isolation (OFF-state)



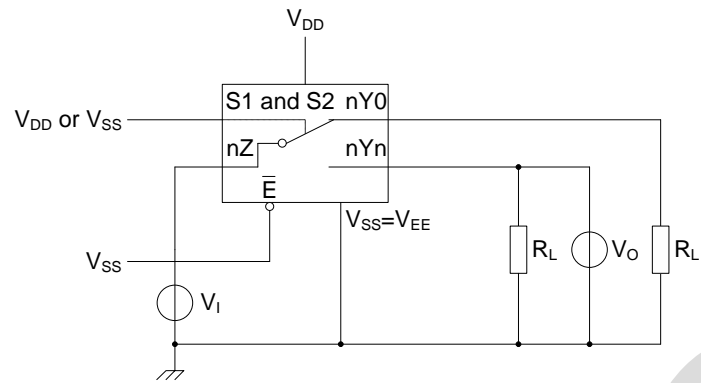
a. Test circuit



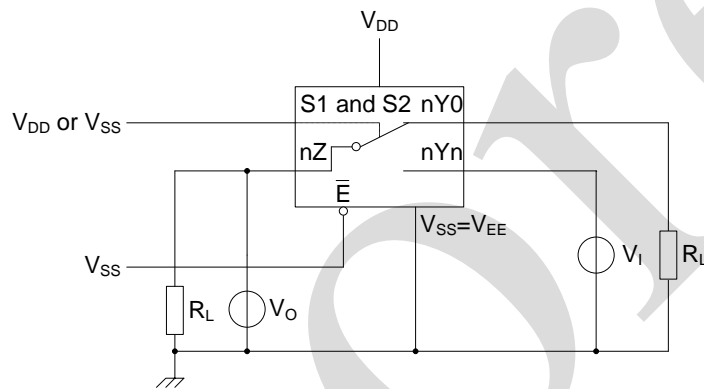
b. Input and output pulse definitions

Figure 17. Test circuit for measuring crosstalk voltage between digital inputs and switch





a. Switch closed condition



b. Switch open condition

Figure 18. Test circuit for measuring crosstalk between switches

#### 4.7、 Measurement Points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5V to 18V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

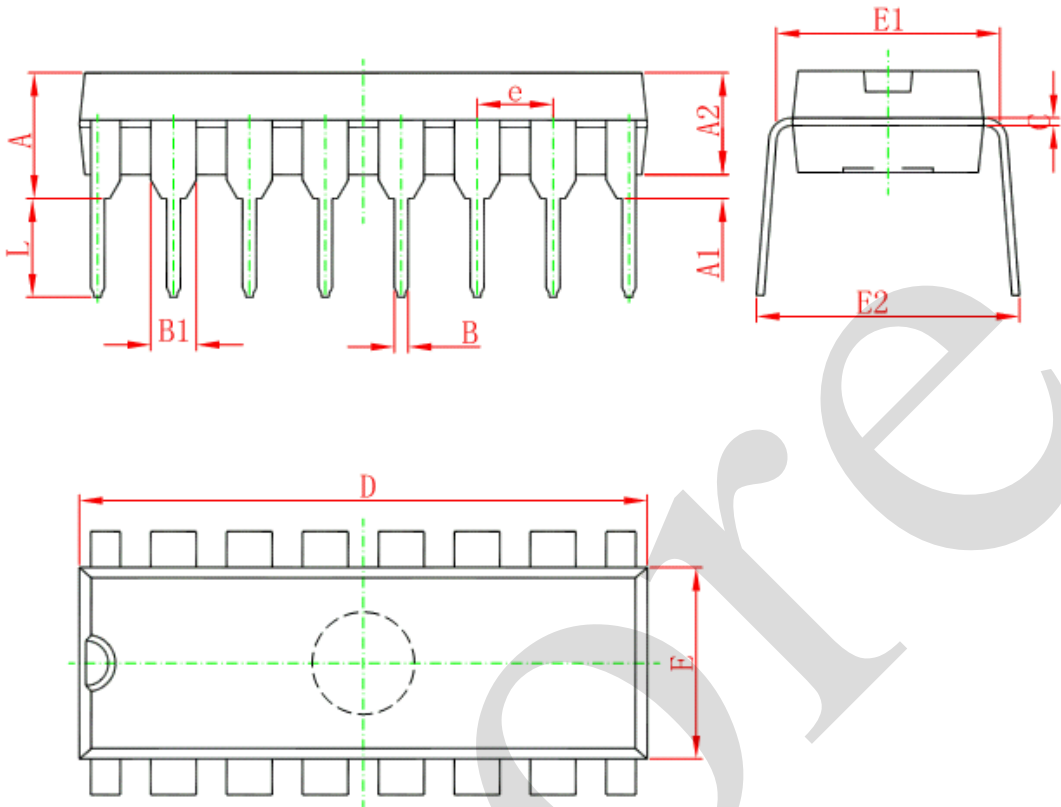
#### 4.8、 Test Data

Input				Load		S1 position				
nYn, nZ	Sn and $\bar{E}$	$t_r, t_f$	$V_M$	$C_L$	$R_L$	$t_{PHL}^{[1]}$	$t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	other
$V_{DD}$ OR $V_{EE}$	$V_{DD}$ OR $V_{SS}$	$\leq 20ns$	$0.5 \times V_{DD}$	50pF	10kΩ	$V_{DD}$ OR $V_{EE}$	$V_{EE}$	$V_{EE}$	$V_{DD}$	$V_{EE}$



## 5、 Package Information

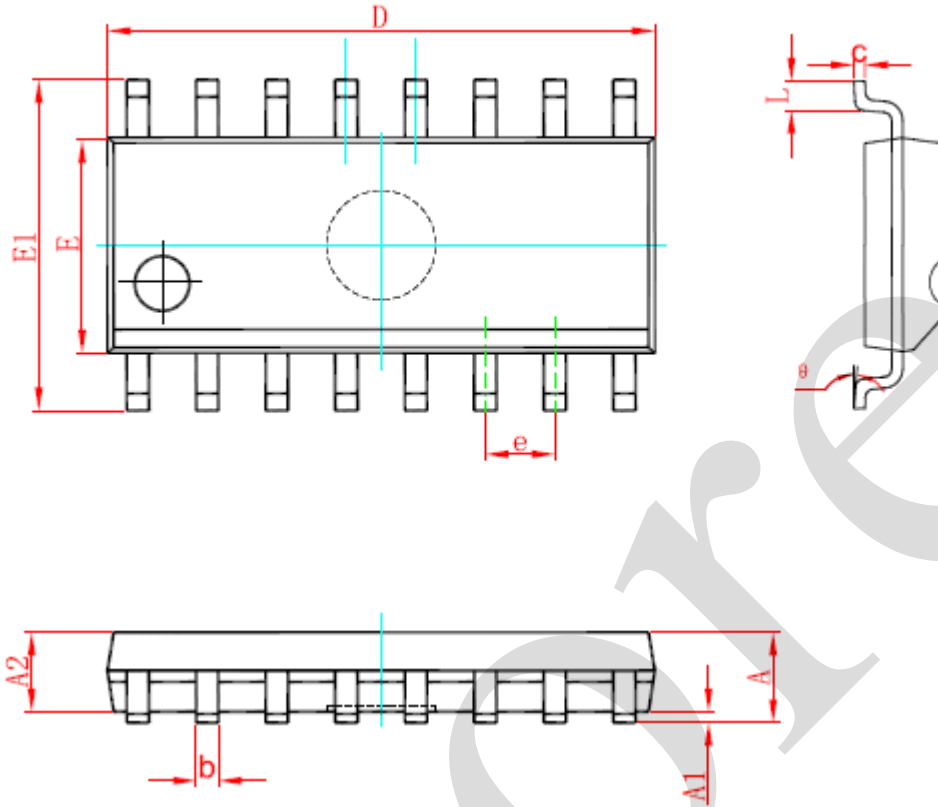
### 5.1、 DIP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354



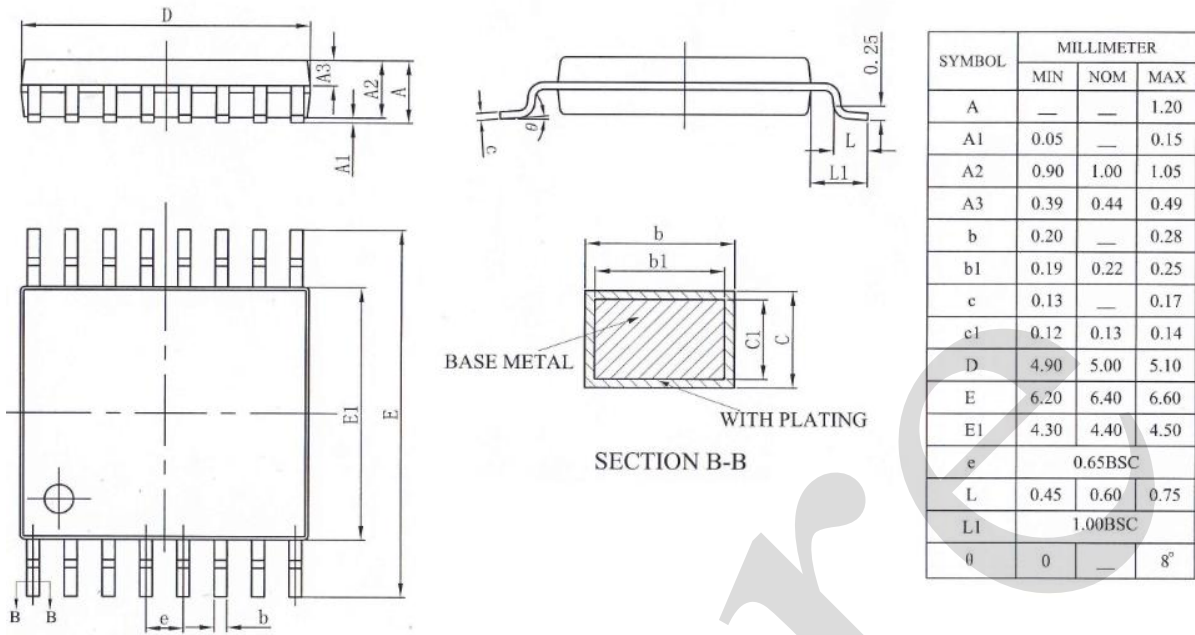
## 5.2、SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



**5.3、TSSOP16**





## 6、 Statements And Notes

### 6.1、 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

### 6.2、 Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.