*Click **here** to ask an associate for production status of specific part numbers.*

MAXM17572

4.5V to 60V, 1A Himalaya uSLIC Step-Down Power Module

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power-supply solutions. The MAXM17572 is a high-efficiency, synchronous, Himalaya step-down DC-DC power module with integrated controller, MOSFETs, compensation components, and inductor that operates over a wide input-voltage range. The module operates from 4.5V to 60V input and delivers up to 1A output current over a programmable output voltage range of 0.9V to 12V. The module significantly reduces design complexity and manufacturing risks, and offers a true “plug-and-play” power supply solution, reducing the time-to-market. The MAXM17572 employs peak-current-mode control architecture.

The MAXM17572 offers programmable switching frequency, $\overline{\text{RESET}}$ output voltage monitoring, adjustable input undervoltage lockout, and programmable soft-start. The module also features hiccup-mode overload protection and a thermal shutdown function.

The MAXM17572 is available in a low-profile, compact, 12-pin 3.5mm x 3.5mm x 2.3mm uSLIC package. Simulation models are available.

Applications

- Industrial Power Supplies
- Distributed Supply Regulation
- FPGA and DSP Point-of-Load Regulator
- Base Station Point-of-Load Regulator
- HVAC and Building Control

Benefits and Features

- Easy to use
  - Wide 4.5V to 60V Input
  - Adjustable 0.9V to 12V Output
  - ±1.2% Feedback Accuracy
  - Up to 1A Output Current
  - Internally Control Loop Compensated
  - All Ceramic Capacitors
- Flexible Design
  - PWM Mode of Operation
  - Adjustable Frequency with External Frequency Synchronization (400kHz to 2.2MHz)
  - Programmable Soft-Start
  - Open-Drain Power Good Output ($\overline{\text{RESET}}$ Pin)
  - Programmable EN/UVLO threshold
  - Auxiliary Bootstrap Supply ($EXTV_{CC}$) for Improved Efficiency
- Robust Operation
  - Over Temperature Protection
  - Hiccup Over Current Protection
  - High Industrial Ambient Operating Temperature Range (-40°C to +125°C)/Junction Temperature Range (-40°C to +150°C)
- Rugged
  - Complies with CISPR32 (EN55032) Class B Conducted and Radiated Emissions.

***Ordering Information** appears at end of data sheet.*

19-101182; Rev 0; 9/21

Typical Application Circuit

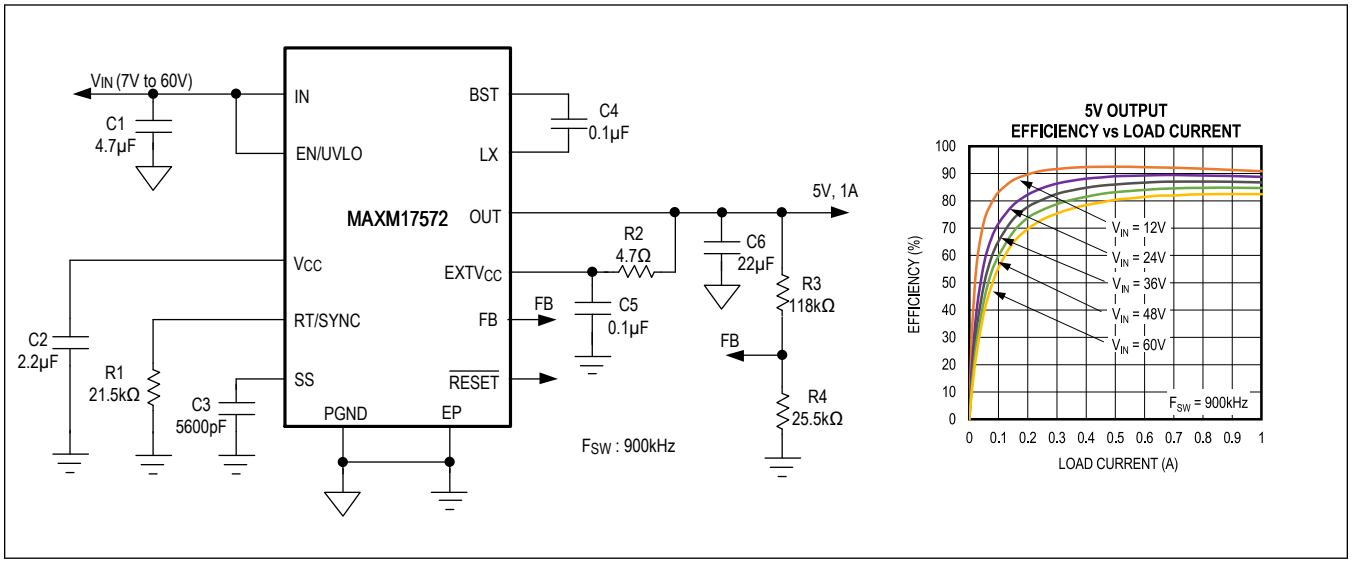


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

IN to PGND ..... -0.3V to +65V
EN/UVLO to SGND ..... -0.3V to +(V_{IN} + 0.3)V
$EXTV_{CC}$ to SGND ..... -0.3V to lower of (V_{IN} + 0.3V)/+26V
BST to PGND ..... -0.3V to +70V
BST to LX ..... -0.3V to +6.0V
BST to V_{CC} ..... -0.3V to +65V
FB to SGND ..... -0.3V to 1.5V
RT/ SYNC, SS, $\overline{RESET}$, V_{CC} to SGND ..... -0.3V to +6.0V
OUT to PGND ..... -0.3V to +(V_{IN} + 0.3)V
PGND to SGND ..... -0.3V to +0.3V
Output Short Circuit Duration ..... Continuous
Operating Temperature Range (Note 1) ..... -40C to +125C
Junction Temperature ..... -40°C to +150°C
Storage Temperature Range ..... -40°C to +125°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature (soldering, 10s) ..... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 PIN uSLIC

Package Code	M123A3+2
Outline Number	21-100356
Land Pattern Number	90-100113
Thermal Resistance Four Layer Board (Note 2)	
Junction to Ambient (θ_{JA})	42°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 2: Package thermal resistance is measured on an evaluation board with no airflow.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2kΩ, C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{EXTVCC} = 0, LX = SS = $\overline{RESET}$ = OUT = OPEN, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted (Note3).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		4.7	7.25	µA
Input Quiescent Current	I_{Q_PWM}	Normal switching mode, V_{FB} = 0.8V		11		mA
Enable/Under Voltage Lockout (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.26	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.131	
EN/UVLO Input Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 1.25V, T_A = 25°C	-50		+50	nA
LDO (V_{CC})						
V_{CC} Output Voltage Range	V_{CC}	6V ≤ V_{IN} ≤ 60V; I_{VCC} = 1mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 7V	25	54	100	mA
V_{CC} Dropout	V_{VCC-DO}	V_{IN} = 4.5V , I_{VCC} = 15mA			0.35	V

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2kΩ, C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{EXTVCC} = 0, LX = SS = $\overline{RESET}$ = OUT = OPEN, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted (Note3).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} UVLO	$V_{VCC-UVR}$	V_{CC} rising	4.05	4.2	4.3	V
	$V_{VCC-UVF}$	V_{CC} falling	3.65	3.8	3.9	
EXT LDO ($EXTV_{CC}$)						
EXTVCC Switch Over Voltage		EXTVCC rising	4.56	4.7	4.84	V
		EXTVCC falling	4.3	4.45	4.6	
EXTVCC Dropout	$EXTV_{CC-DO}$	V_{EXTVCC} = 4.75V , I_{EXTVCC} = 15mA			0.3	V
EXTVCC Current Limit	$EXTVCC\_C_{ILIM}$	V_{VCC} = 4.5V, V_{EXTVCC} = 7V	26.5	60	105	mA
SOFT-START (SS)						
Soft Start Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		2.05	2.47	2.8	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		2.5	2.76	3.1	A
OUTPUT SPECIFICATIONS						
FB Regulation Voltage	V_{FB_REG}		0.889	0.9	0.911	V
FB Input Bias Current	I_{FB}	0V ≤ V_{FB} ≤ 1V, T_A = +25°C	-50		+50	nA
FB Undervoltage Trip Level to Cause HICCUP	$V_{FB-HICF}$		0.56	0.58	0.65	V
HICCUP Timeout		(Note 4)		32768		Cycles
RT/SYNC and Timings						
Switching Frequency	F_{SW}	R_{RT} = OPEN	430	490	550	kHz
		R_{RT} = 51.1kΩ	370	400	430	
		R_{RT} = 40.2kΩ	475	500	525	
		R_{RT} = 8.06kΩ	1950	2200	2450	
Synchronization Frequency Capture Range		F_{SW} set by R_{RT}	1.1 x F_{SW}		1.4 x F_{SW}	
Synchronization Pulse Width			50			ns
Synchronization Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
Minimum On-Time	t_{ON_MIN}			60	80	ns
Minimum Off-Time	t_{OFF_MIN}		140	150	160	ns
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output Leakage Current		T_A = T_J = +25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2kΩ, C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{EXTVCC} = 0, LX = SS = $\overline{RESET}$ = OUT = OPEN, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted (Note3).)

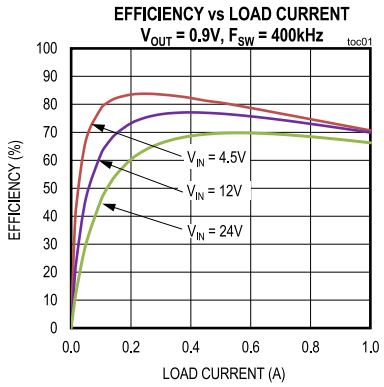
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB} Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.5	92	94.6	%
V_{FB} Threshold for $\overline{RESET}$ De-assertion	V_{FB-OKR}	V_{FB} rising	93.8	95	97.8	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDNR}	Temp rising		165		ºC
Thermal Shutdown Hysteresis	T_{SHDNHY}			10		ºC

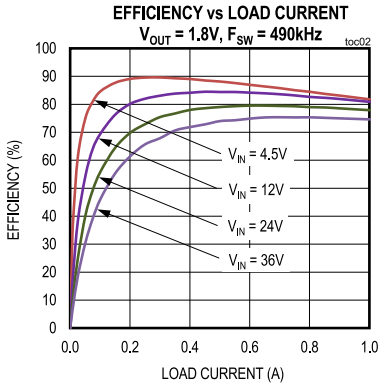
Note 2: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

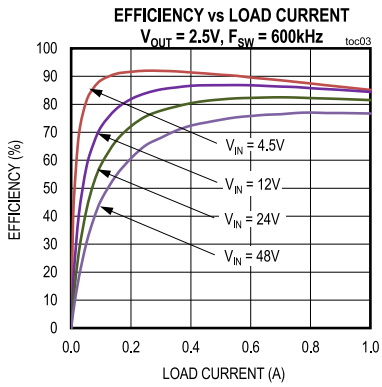
Note 3: See the *Overcurrent Protection / Hiccup Mode* section for more details

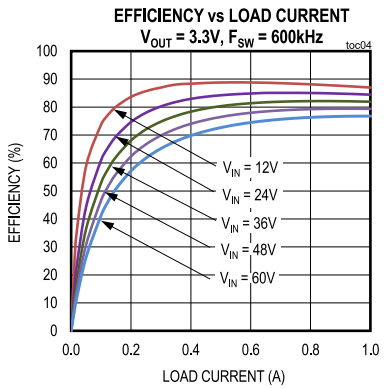
Typical Operating Characteristics

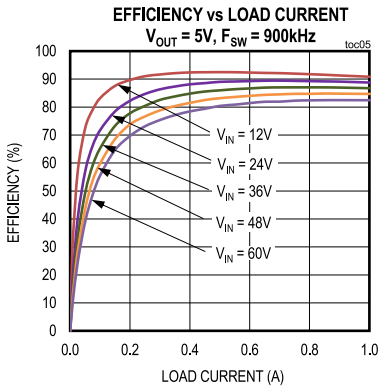
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications shown in Table 2, unless otherwise noted.)

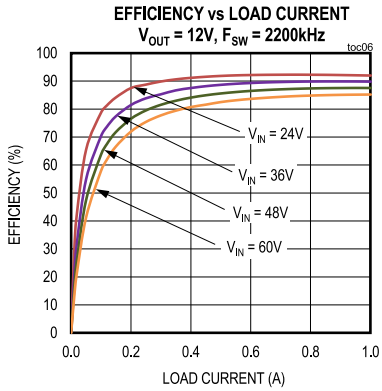


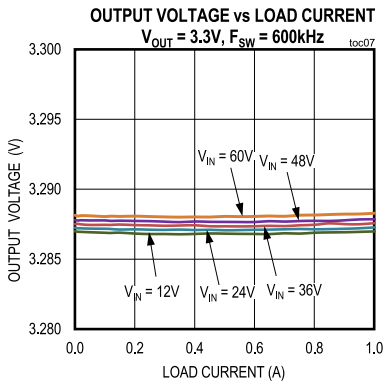


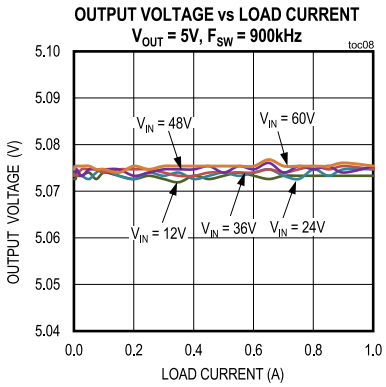


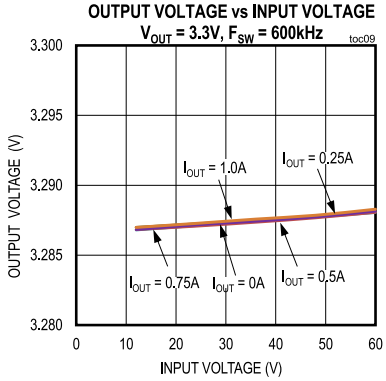






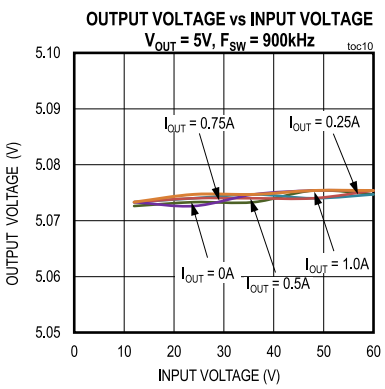


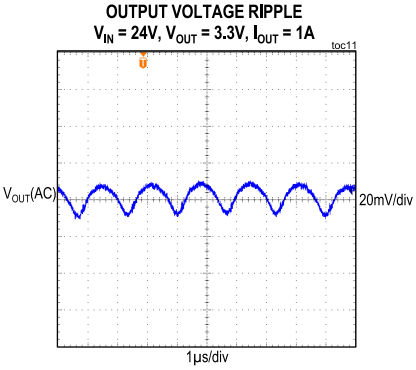


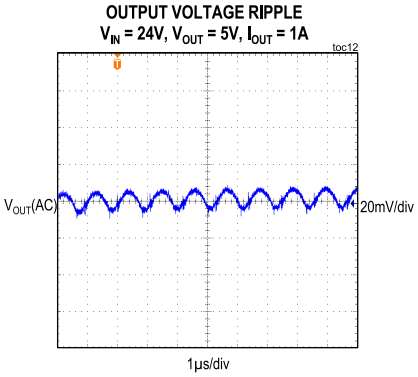


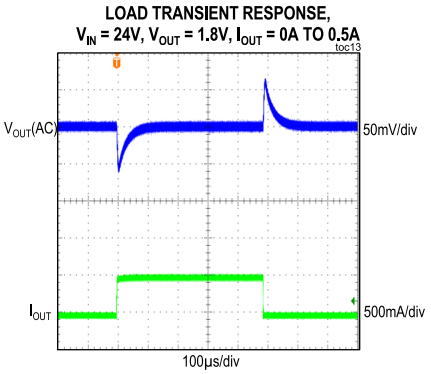
Typical Operating Characteristics (continued)

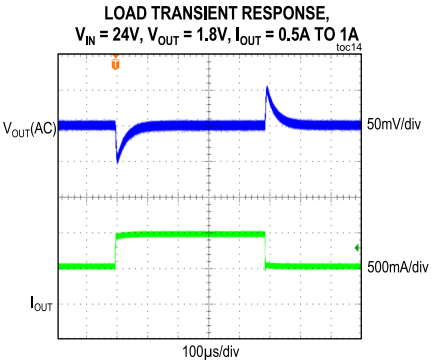
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications shown in Table 2, unless otherwise noted.)

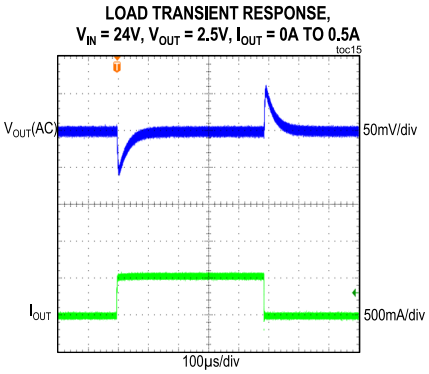


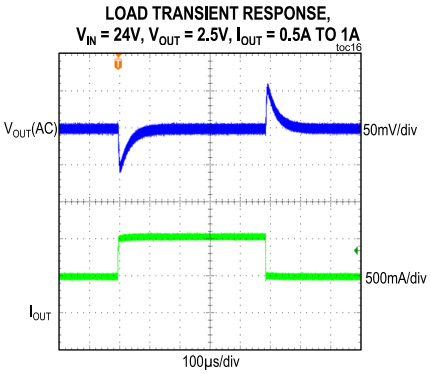


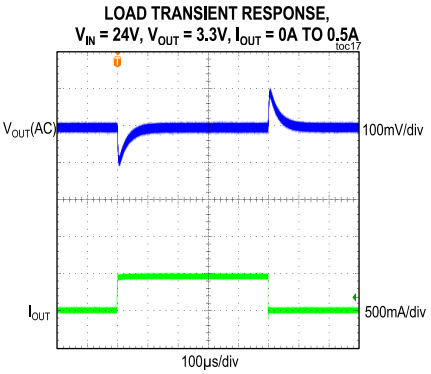


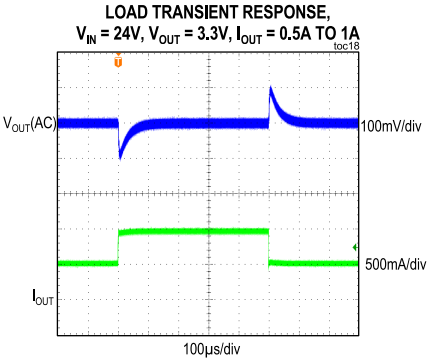








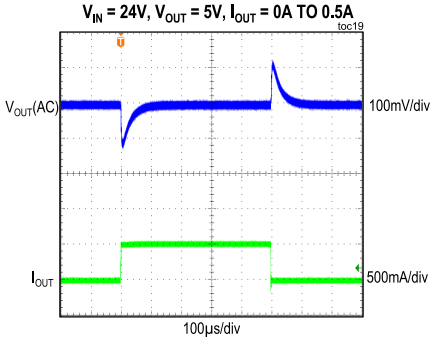




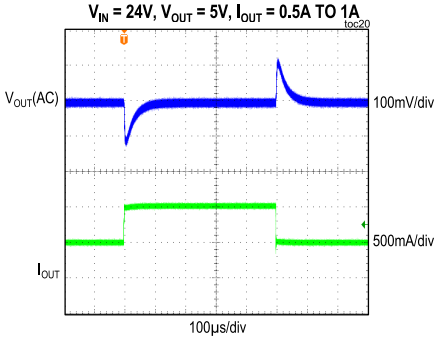
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications shown in Table 2, unless otherwise noted.)

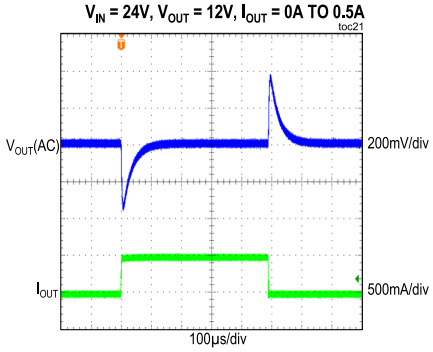
LOAD TRANSIENT RESPONSE,
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0A TO 0.5A



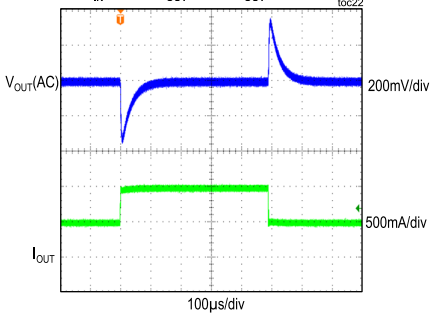
LOAD TRANSIENT RESPONSE,
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.5A TO 1A



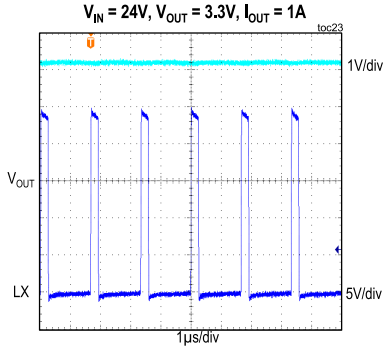
LOAD TRANSIENT RESPONSE,
V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 0A TO 0.5A



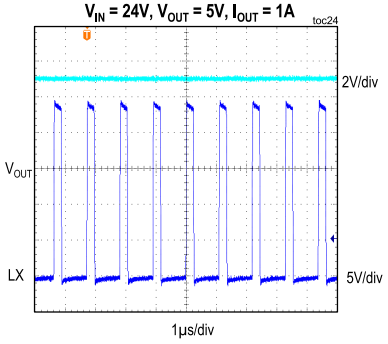
LOAD TRANSIENT RESPONSE,
V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 0.5A TO 1A



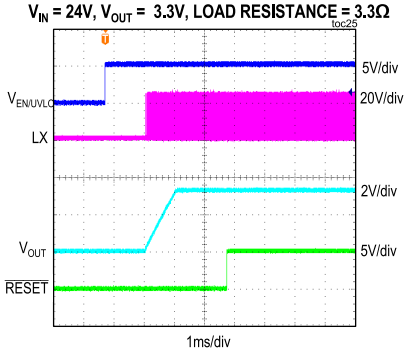
STEADY STATE LX AND OUTPUT VOLTAGE
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A



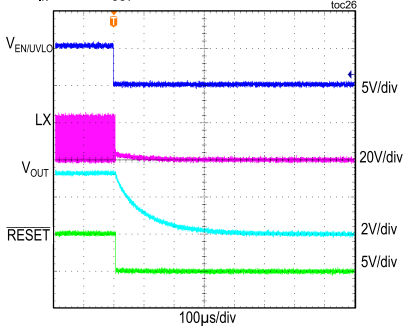
STEADY STATE LX AND OUTPUT VOLTAGE
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A



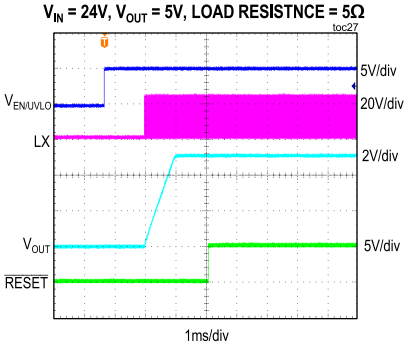
STARTUP THROUGH ENABLE
V_{IN} = 24V, V_{OUT} = 3.3V, LOAD RESISTANCE = 3.3Ω



SHUTDOWN THROUGH ENABLE
V_{IN} = 24V, V_{OUT} = 3.3V, LOAD RESISTANCE = 3.3Ω



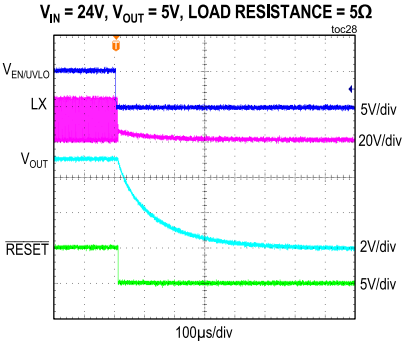
STARTUP THROUGH ENABLE
V_{IN} = 24V, V_{OUT} = 5V, LOAD RESISTNCE = 5Ω



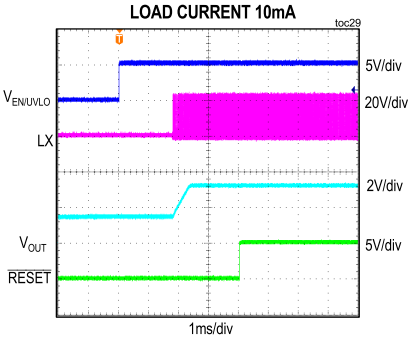
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications shown in Table 2, unless otherwise noted.)

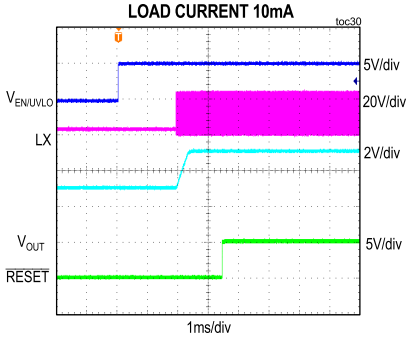
SHUTDOWN THROUGH ENABLE
V_{IN} = 24V, V_{OUT} = 5V, LOAD RESISTANCE = 5Ω



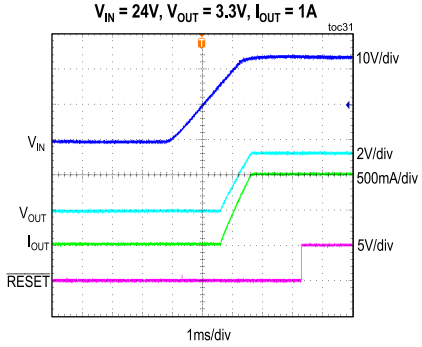
STARTUP WITH 1.5V PREBIAS 3.3V OUTPUT
LOAD CURRENT 10mA



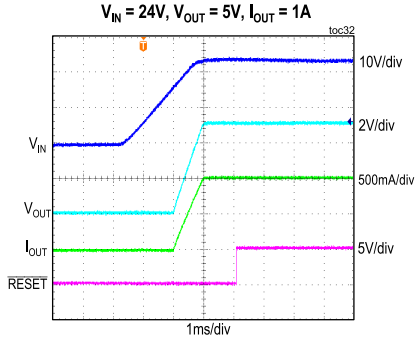
STARTUP WITH 2.5V PREBIAS 5V OUTPUT
LOAD CURRENT 10mA



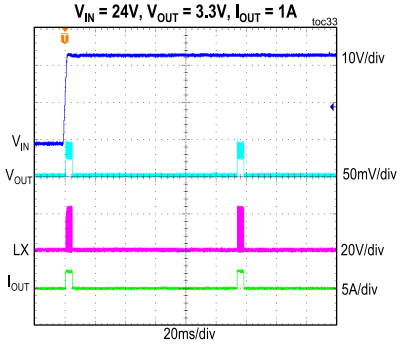
STARTUP THROUGH INPUT SUPPLY
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A



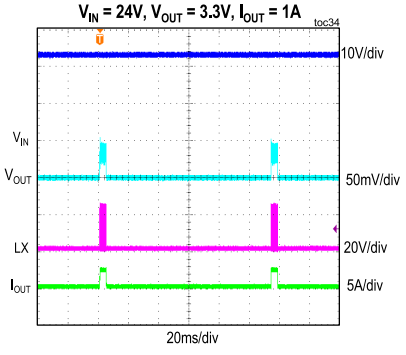
STARTUP THROUGH INPUT SUPPLY
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A



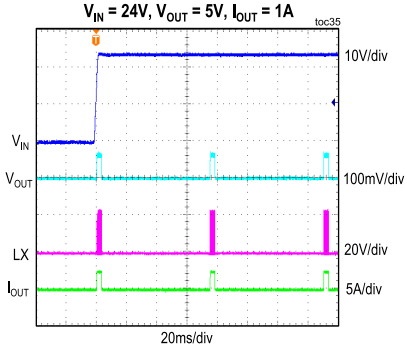
OUTPUT SHORT DURING STARTUP
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A



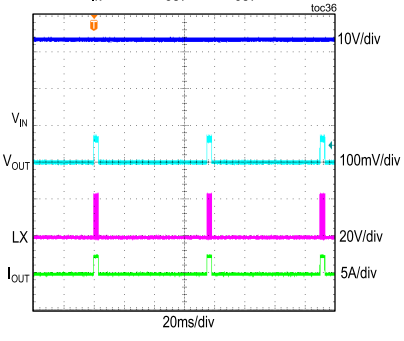
OUTPUT SHORT IN STEADY STATE
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A



OUTPUT SHORT DURING STARTUP
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A



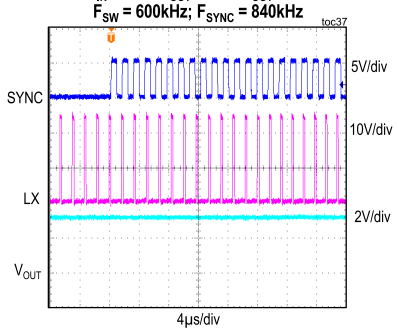
OUTPUT SHORT IN STEADY STATE
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A



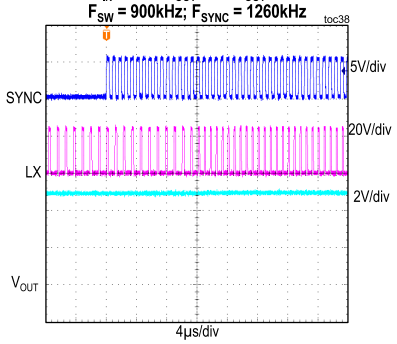
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications shown in Table 2, unless otherwise noted.)

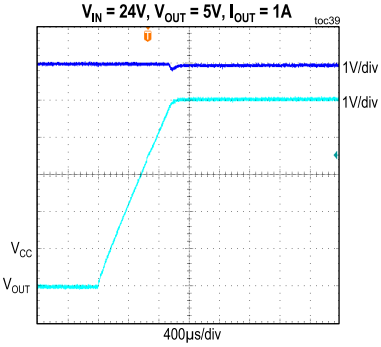
EXTERNAL SYNCHRONIZATION
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A
F_{SW} = 600kHz; F_{SYNC} = 840kHz



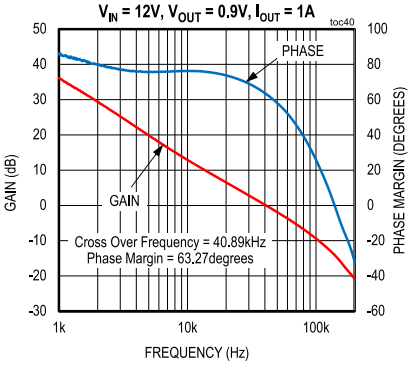
EXTERNAL SYNCHRONIZATION
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A
F_{SW} = 900kHz; F_{SYNC} = 1260kHz



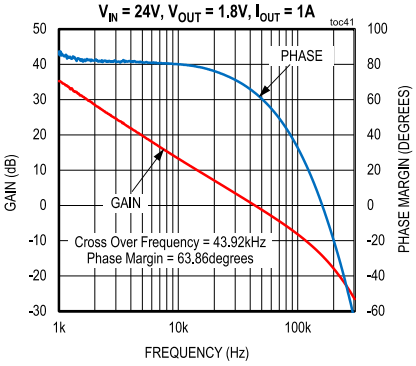
EXTVCC SWITCHOVER VOLTAGE
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A



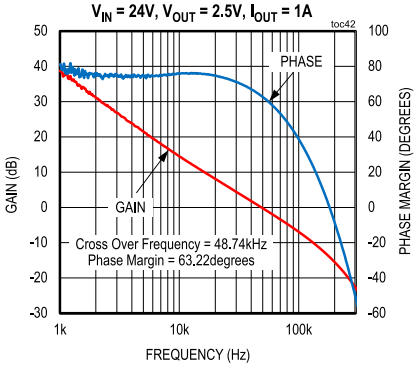
BODE PLOT
V_{IN} = 12V, V_{OUT} = 0.9V, I_{OUT} = 1A



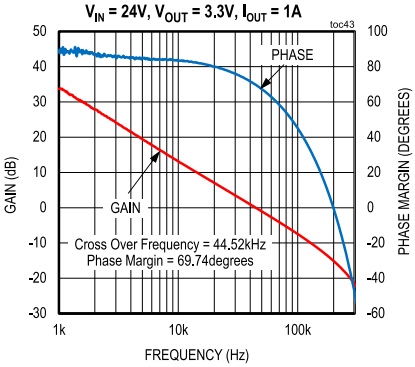
BODE PLOT
V_{IN} = 24V, V_{OUT} = 1.8V, I_{OUT} = 1A



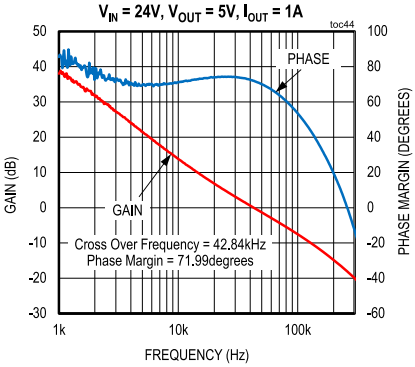
BODE PLOT
V_{IN} = 24V, V_{OUT} = 2.5V, I_{OUT} = 1A



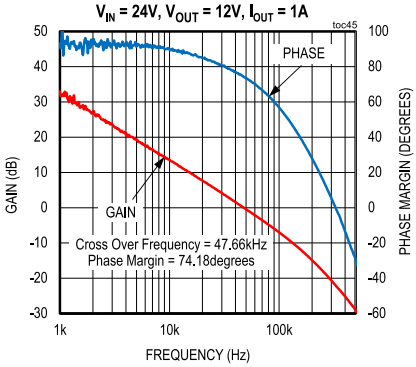
BODE PLOT
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1A



BODE PLOT
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A

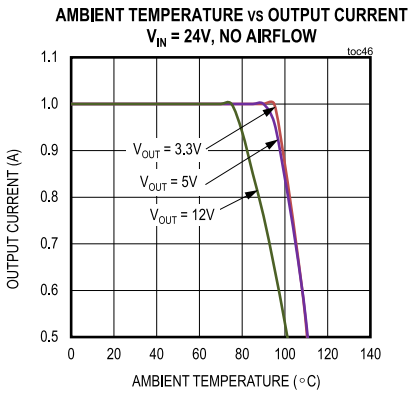


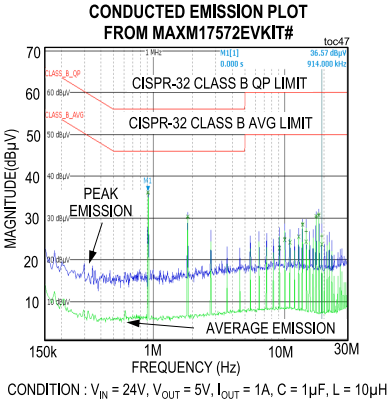
BODE PLOT
V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A

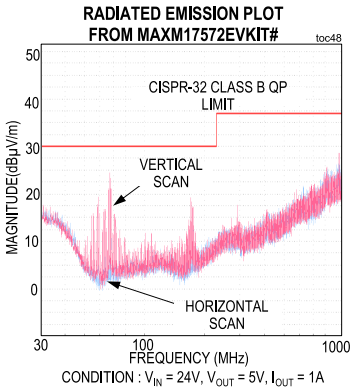


Typical Operating Characteristics (continued)

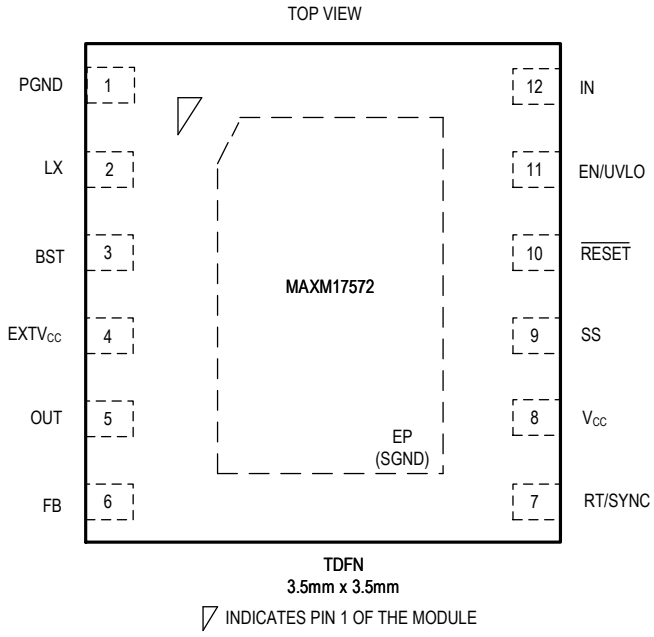
(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{SGND} = 0V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted. The circuit values for different output-voltage applications shown in Table 2, unless otherwise noted.)







Pin Configuration



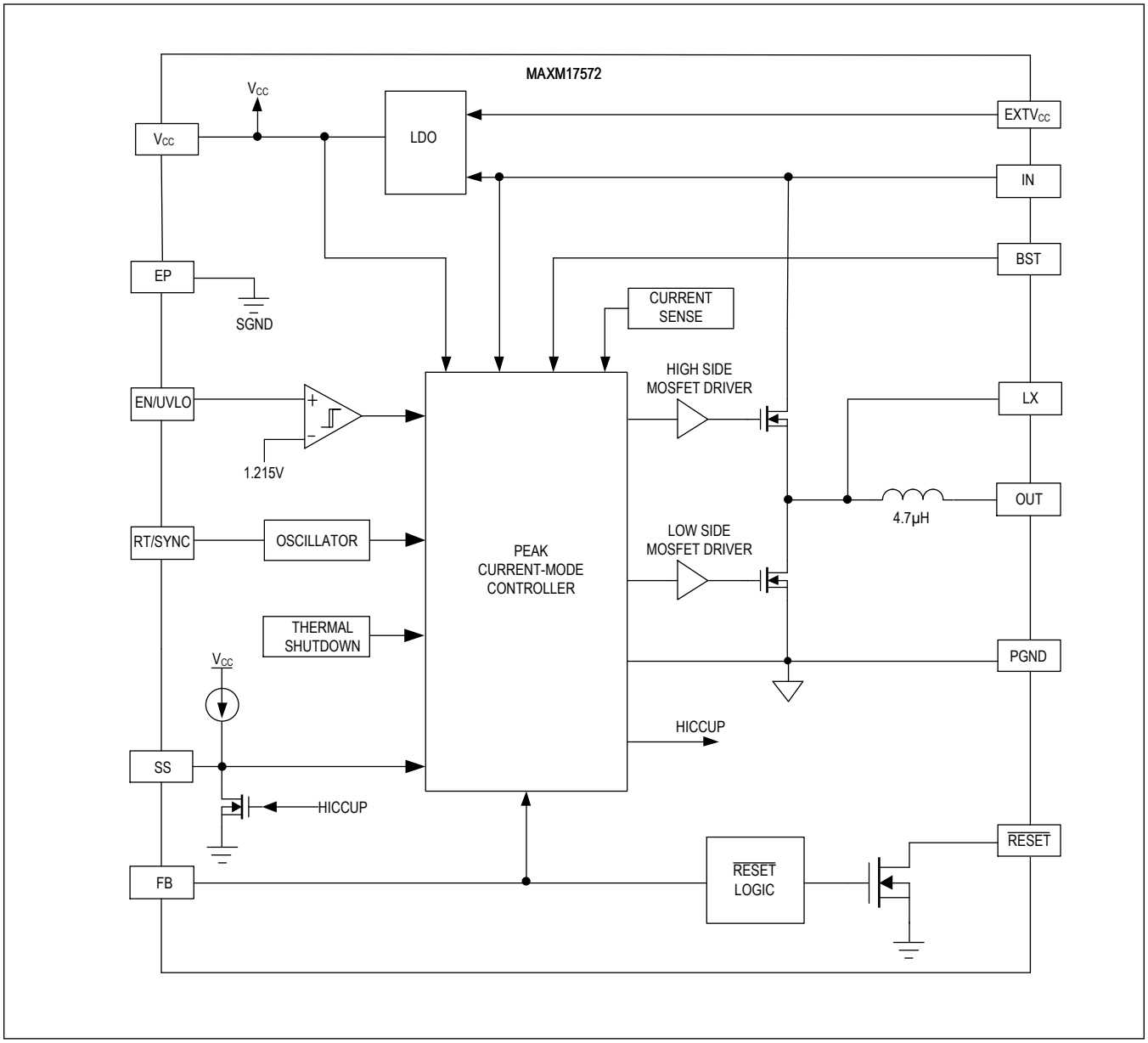
Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground Pin. Connect the PGND pin externally to the power ground plane.

Pin Description (continued)

PIN	NAME	FUNCTION
2	LX	Switching node of the inductor.
3	BST	Bootstrap capacitor node.Connect a 0.1µF ceramic capacitor between BST and LX.
4	$EXTV_{CC}$	External Power Supply Input. Reduces the Internal-LDO Loss. Connect it to OUT when output voltage is programmed between 5V to 12V. When $EXTV_{CC}$ is not used, connect it to SGND.
5	OUT	Module Output Pin. Connect a capacitor from OUT to PGND. See the *PCB Layout Guidelines* section for more details.
6	FB	Output Feedback Connection. Connect FB to a resistor-divider between OUT and SGND to set the output voltage.
7	RT/SYNC	Oscillator Timing Resistor Input. Connect a resistor from RT/SYNC to SGND to program the switching frequency from 400kHz to 2.2MHz. Leave RT/SYNC open for the default 490 kHz frequency. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency. See the *Setting the Switching Frequency (RT)* and *External Frequency Synchronization (SYNC)* sections for details.
8	V_{CC}	5V LDO Output of the module. Bypass V_{CC} with a 2.2µF ceramic capacitor to SGND.
9	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
10	$\overline{RESET}$	Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low if FB drops below 92% of its set value. $\overline{RESET}$ goes high 1024 clock cycles after FB rises above 95% of its set value.
11	EN/UVLO	Enable/Under Voltage Lockout Input. Pull EN/UVLO to SGND to disable the module output. Connect EN/UVLO to IN for always-ON operation. Connect a resistor-divider between IN, EN/UVLO, and SGND to program the input voltage at which the module turns on.
12	IN	Power Supply Input. Decouple to PGND with a capacitor; place the capacitor close to IN and PGND pins.
-	EP	Exposed Pad and Signal Ground (SGND). Connect a large copper plane below the module to improve heat dissipation capability. Add thermal vias below the exposed pad. Refer to the MAXM17572 EV kit datasheet for a layout example.

Functional Block Diagrams



Detailed Description

The MAXM17572 is a high-efficiency, synchronous, step-down DC-DC power module with integrated controller, MOSFETs, compensation components, and inductor that operates over a wide input-voltage range. The module operates from 4.5V to 60V input and delivers up to 1A output current over a programmable output voltage range of 0.9V to 12V. When EN/UVLO and the V_{CC} threshold are ascertained to be higher than their respective rising threshold levels, an internal power-up sequence ramps up the error-amplifier reference, resulting in an output-voltage soft-start.

The FB pin monitors the output voltage through a resistor divider. The $\overline{RESET}$ pin transitions to a high-impedance state 1024 clock cycles after the output voltage reaches 95% of regulation. The module operates in pulse-width modulation (PWM) mode providing a constant frequency operation at all loads. The module features a RT/SYNC pin to program the switching frequency. A programmable soft-start feature allows users to reduce input inrush current. The module also incorporates an input enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the module at the desired input-voltage level.

The module employs a peak-current-mode control architecture. An internal error amplifier compares the feedback voltage to a fixed reference voltage and generates an error voltage. The error voltage is compared to the sum of the current-sense voltage and slope-compensation voltage by a PWM comparator to set the on-time. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the internal inductor current ramps up. During the rest of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor in the module releases the stored energy as its current ramps down and provides current to the output.

Linear Regulator (V_{CC}, $EXTV_{CC}$)

The module has two internal low-dropout regulators (LDOs) that power V_{CC}. One LDO is powered from IN and the other LDO is powered from $EXTV_{CC}$. Only one of the two LDOs is in operation at a time, depending on the voltage levels present at $EXTV_{CC}$. If $EXTV_{CC}$ voltage is greater than 4.7V (typ), V_{CC} is powered from $EXTV_{CC}$. If $EXTV_{CC}$ is lower than 4.7V (typ), V_{CC} is powered from IN. Powering V_{CC} from $EXTV_{CC}$ increases efficiency at higher input voltages. $EXTV_{CC}$ voltage should not exceed (V_{IN} + 0.3) and 26V.

Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver, and recharges the external bootstrap capacitor. The MAXM17572 employs an undervoltage-lockout circuit that forces both the regulators off when V_{CC} falls below 3.8V (typ). The regulators can be immediately enabled again when V_{CC} is higher than 4.2V (typ). The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck converter output is connected to the $EXTV_{CC}$ pin, if the output is shorted to ground, then transfer from $EXTV_{CC}$ LDO to the internal LDO happens seamlessly without any impact on the normal functionality.

Enable/Undervoltage Lockout (EN/UVLO), Soft-Start (SS)

When EN/UVLO voltage is above 1.215V (typ), the internal error-amplifier reference voltage of the module starts to ramp up. The duration of the soft-start ramp is programmable through the choice of an external capacitor put at the SS pin, allowing a smooth increase of the output voltage. Driving EN/UVLO low disables both power MOSFETs as well as other internal circuitry and reduces IN shutdown current to below 4.7µA (typ). EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between IN and EN/UVLO to SGND adjusts the input voltage at which the module turns on or turns off. If input UVLO programming is not desired, connect EN/UVLO to IN (see the *Electrical Characteristics* table for EN/UVLO rising and falling threshold voltages).

External Frequency Synchronization (SYNC)

The internal oscillator of the MAXM17572 can be synchronized to an external clock signal through the RT/ SYNC pin. The external clock should be coupled to the RT/SYNC pin using the circuit as shown in Figure 1. The external synchronization clock frequency must be between 1.1 × F_{SW} and 1.4 × F_{SW}, where F_{SW} is the frequency programmed by the RT resistor (R_{RT}). A resistor must be connected from the RT/SYNC pin to GND to be able to synchronize the MAXM17572 to an external clock. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to the external clock frequency (from the original frequency based on the RT setting) after detecting 16 external clock edges. The minimum external clock high pulse width and amplitude should be greater than 50ns and 2.1V, respectively. The

maximum external clock low pulse amplitude should be less than 0.8V.

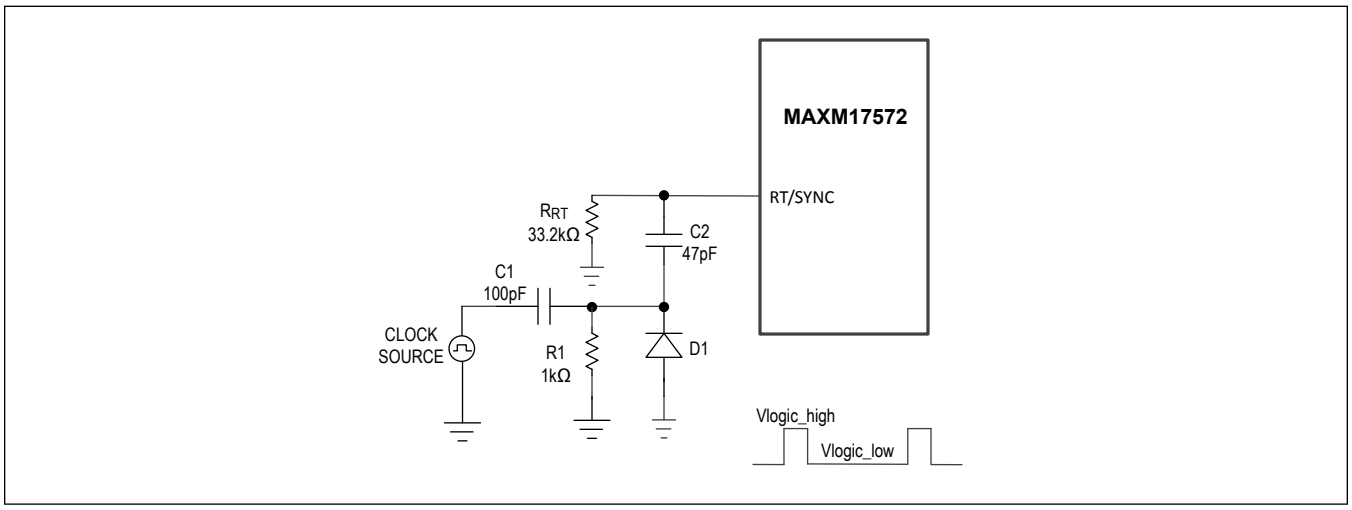


Figure 1. External Clock Synchronization

$\overline{\text{RESET}}$ Output

The module includes a $\overline{\text{RESET}}$ pin to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pull-up resistor. $\overline{\text{RESET}}$ goes high impedance 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops below 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Startup into Prebiased Output

The module is capable of soft-start into a prebiased output, without discharging the output capacitor. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

Overcurrent Protection/Hiccup Mode

The module is provided with a robust overcurrent protection (OCP) scheme that protects the module under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of $I_{PEAK-LIMIT}$ (2.47A typ). A runaway current limit on the high-side switch current at the $I_{RUNAWAY-LIMIT}$ (2.76A typ) protects the device under high input voltage and output short circuit conditions when there is insufficient output voltage available to restore the module current that was built up during the on period of the module. One occurrence of the runaway current limit triggers hiccup mode. In addition, hiccup mode is activated if the feedback voltage drops below 64.5% of the nominal value any time after soft-start is completed due to any fault. In hiccup mode, the module is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload condition, if feedback voltage does not exceed 64.5% of the nominal value, the modules continue to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

The MAXM17572 is designed to support a maximum load current of 1A. The inductor ripple current is calculated as follows:

$$\Delta I = \left[\frac{V_{IN} - V_{OUT} - I_{OUT} \times 0.74}{L \times F_{SW}}\right] \times \left[\frac{V_{OUT} + I_{OUT} \times 0.44}{V_{IN} - I_{OUT} \times 0.30}\right]$$

Where

V_{OUT} = Steady state output voltage

V_{IN} = Operating input voltage

F_{SW} = Switching Frequency in Hz

L = Power module output inductance (4.7µH ±20%)

I_{OUT} = Required output (load) current

The following condition should be satisfied at the desired load current, I_{OUT}:

$$I_{OUT} + \frac{\Delta I}{2} < 2.05$$

Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the module. When the junction temperature exceeds +165°C, an on-chip thermal sensor shuts down the module and turns off the internal power MOSFETs, allowing the module to cool down. The thermal sensor turns the module on after the junction temperature cools by 10°C.

Applications Information

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = (I_{OUT} \times 0.3) + \frac{V_{OUT} + (I_{OUT} \times 0.44)}{1 - (F_{SW(MAX)} \times t_{OFF\_MIN(MAX)})}$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{F_{SW(MAX)} \times t_{ON\_MIN(MAX)}}$$

Where

V_{OUT} = Steady-state output voltage

I_{OUT} = Maximum load current

$F_{SW(MAX)}$ = Worst-case switching frequency in Hz

$t_{OFF\_MIN(MAX)}$ = Worst case minimum OFF time (160ns)

$t_{ON\_MIN(MAX)}$ = Worst case minimum ON time (80ns)

For D > 0.5, $V_{IN(MIN)} = 3.09 \times V_{OUT} + 1.66 \times I_{OUT} - \frac{5.80 \times 10^{-3} \times F_{SW}}{500}$

Where F_{SW} = Switching frequency in Hz

Selection of Input Capacitor

The input capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the switching of the module. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Where $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so:

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times \Delta V_{IN} \times F_{SW}}$$

Where

D is the operating duty cycle of the converter

ΔV_{IN} is the allowable input voltage ripple

F_{SW} is the operating switching frequency in Hz

η is the efficiency of the converter

In applications where the source is located away and distant from the device input, an appropriate electrolytic capacitor should be added to provide necessary damping of potential oscillations caused by the inductance of the input power path and input ceramic capacitor.

Selection of Output Capacitor

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The minimum recommended output capacitor values are listed in Table 1 for desired output voltages to support a dynamic step load of 50% of the maximum output current and to contain the output-voltage deviation to 3% of the output voltage. For additional adjustable output voltages and dynamic step load, the required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$t_{RESPONSE} \approx \frac{0.33}{f_C}$$

Where

C_{OUT} is the required output capacitance

ΔV_{OUT} is the allowable output voltage deviation

I_{STEP} is the load current step

$t_{RESPONSE}$ is the response time of the controller

Select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 495kHz. If the switching frequency is more than 495kHz, select f_C to be 55kHz. Derating of ceramic capacitors with DC-voltage at appropriate AC voltage (equal to the steady-state output voltage ripple) must be considered when selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Selection of Soft-Start Capacitor

The module implements an adjustable soft-start operation to reduce inrush current during startup. A capacitor (C_{SS}) connected from the SS pin to SGND to program the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum value of C_{SS}, as shown by the following equation:

$$C_{SS} \geq 56 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that during start-up, the module operates at half the programmed switching frequency until the output voltage reaches 66.7% of set output nominal voltage.

Setting the Input Undervoltage-Lockout Level

The module offers an adjustable input undervoltage-lockout level. Set the voltage at which the module turns on with a resistive voltage-divider connected from IN to SGND (see Figure 2). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ (max) and then calculate R2 as follows:

$$R_2 = \frac{R_1 \times 1.215}{V_{INU} - 1.215}$$

where V_{INU} is the voltage at which the module is required to turn on. See Table 1 to set the proper V_{INU} voltage greater than or equal to the minimum input voltage for each desired output voltage.

If the EN/UVLO pin is driven from an external signal source, it is recommended to place a series resistance of 1kΩ minimum between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

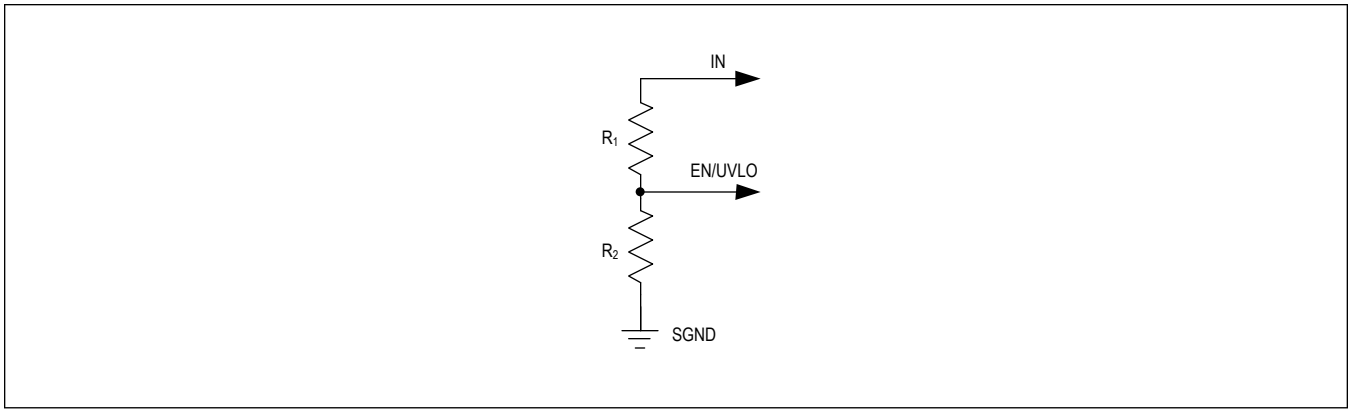


Figure 2. Setting the Input Undervoltage Lockout

Setting the Output Voltage

Set the output voltage with resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 3). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_U from the output to the FB pin using the equation below:

$$R_U = \frac{85}{f_C \times C_{OUT}}$$

Where

C_{OUT} (in F) is the actual derated value of the output capacitance used

R_U is in kΩ

The minimum allowable value of R_U (in kΩ) is ($5.6 \times V_{OUT}$). If the value of R_U calculated using the previous equation is less than ($5.6 \times V_{OUT}$), increase the value of R_U to at least ($5.6 \times V_{OUT}$).

Use the following equation to calculate the R_B:

$$R_B = \frac{R_U \times 0.9}{V_{OUT} - 0.9}$$

Where R_B is in kΩ.

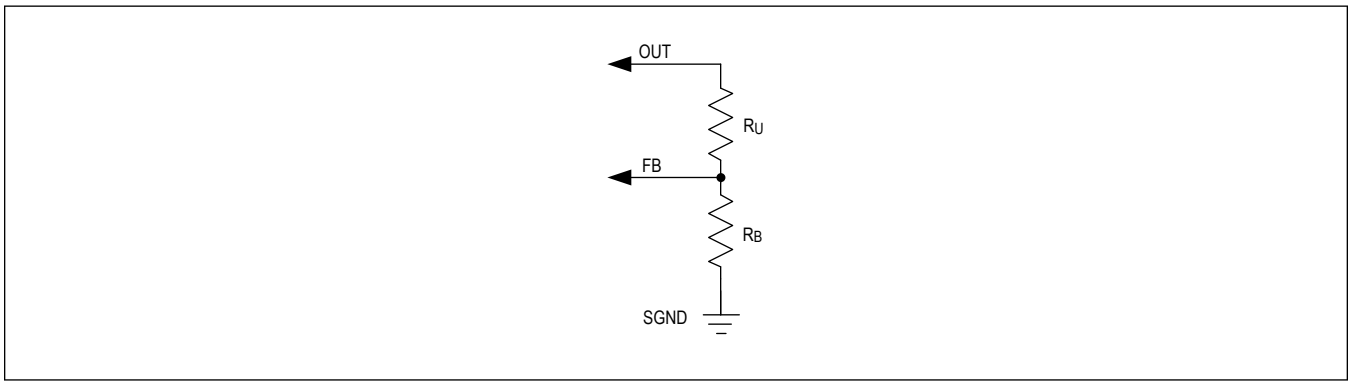


Figure 3. Adjusting Output Voltage

Setting the Switching Frequency (RT)

The switching frequency of the module can be programmed from 400kHz to 2.2MHz by using a resistor connected from

the RT/SYNC pin to SGND. The switching frequency (F_{SW}) is related to the resistor (R_{RT}) connected at the RT/SYNC pin by the following equation:

$$R_{RT} \approx \frac{21 \times 10^6}{F_{SW}} - 1.7$$

where R_{RT} is in kΩ and F_{SW} is in Hz. Leave the RT/SYNC pin open to operate at the default switching frequency of 490kHz. See Table 1 for R_{RT} resistor values for a few common switching frequencies.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
400	51.1
490	OPEN
1000	19.1
2200	8.06

Selection of Component Values

Table 2. Selection of Component Values

$V_{IN(MIN)}$ (V)	$V_{IN(MAX)}$ (V)	V_{OUT} (V)	C_{IN}	C_{OUT}	R_U (kΩ)	R_B (kΩ)	F_{SW} (kHz)	R_{RT} (kΩ)
4.5	26	0.9	1 x 10µF/50V, 1206 TDK C3216X7R1H106K	2 x 47µF/6.3V, 1210 Murata GRM32ER70J476K	27.4	OPEN	400	51.1
4.5	29	1	1 x 10µF/50V, 1206 TDK C3216X7R1H106K	2 x 47µF/6.3V, 1210 Murata GRM32ER70J476K	28	249	400	51.1
4.5	31	1.2	1 x 10µF/50V, 1206 TDK C3216X7R1H106K	2 x 47µF/6.3V, 1210 Murata GRM32ER70J476K	28	84.5	450	45.3
4.5	34	1.5	1 x 10µF/50V, 1206 TDK C3216X7R1H106K	1 x 47µF/6.3V, 1210 Murata GRM32ER70J476K	60.4	90.9	490	OPEN
4.5	40	1.8	1 x 10µF/50V, 1206 TDK C3216X7R1H106K	1 x 47µF/6.3V, 1210 Murata GRM32ER70J476K	54.9	54.9	490	OPEN
4.5	48	2.5	1 x 4.7µF/100V, 1206 Murata GRM31CZ72A475K	1 x 47µF/6.3V, 1210 Murata GRM32ER70J476K	56.2	31.6	600	33.2
5	60	3.3	1 x 4.7µF/100V, 1206 Murata GRM31CZ72A475K	1 x 22µF/25V, 1210 Murata GRM32ER71E226K	110	41.2	600	33.2
7	60	5	1 x 4.7µF/100V, 1206 Murata GRM31CZ72A475K	1 x 22µF/25V, 1210 Murata GRM32ER71E226K	118	25.5	900	21.5
12	60	8	1 x 1µF/100V, 1206 AVX 12061C105KAT2A	1 x 10µF/16V, 1206 Murata GCM31CR71C106K	309	39.2	1500	12.4
21	60	12	1 x 1µF/100V, 1206 AVX 12061C105KAT2A	1 x 10µF/16V, 1206 Murata GCM31CR71C106K	392	31.6	2200	8.06

Power Dissipation and Output-Current Derating

The power dissipation inside the module leads to an increase in the junction temperature of the MAXM17572. The power loss inside the module at full load can be estimated as follows:

$$P_{LOSS} = P_{OUT} \times [\frac{1}{\eta} - 1]$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

Where

P_{OUT} is the output power of the module

η is the efficiency of the power module at the desired operating conditions

See the *Typical Operating Characteristics* for the power-conversion efficiency or measure the efficiency to determine the total power dissipation. An EE-Sim model is available for the MAXM17572 to simulate efficiency and power loss for the desired operating conditions. The junction temperature (T_J) of the module can be estimated at any given maximum ambient temperature (T_A) from the following equation:

$T_J = T_A + [\theta_{JA} \times P_{LOSS}]$

Where θ_{JA} is the junction to ambient thermal resistance. For the MAXM17572 evaluation board, the thermal resistance from junction-to-ambient (θ_{JA}) is 42°C/W. Operating the module at junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. Use the following guidelines for good PCB layout:

- Keep the input capacitors as close as possible to the IN and PGND pins
- Keep the output capacitors as close as possible to the OUT and PGND pins
- Keep the resistive feedback divider as close as possible to the FB pin
- Connect all of the PGND connections to a copper plane area as large as possible on the bottom layer
- Connect EP to SGND plane on bottom layer
- Use multiple vias to connect internal PGND planes to the top layer PGND plane
- Do not keep any solder mask on EP on bottom layer. Keeping solder mask on exposed pads decreases the heat dissipating capability
- Refer to the MAXM17572 EV kit layout for first pass success

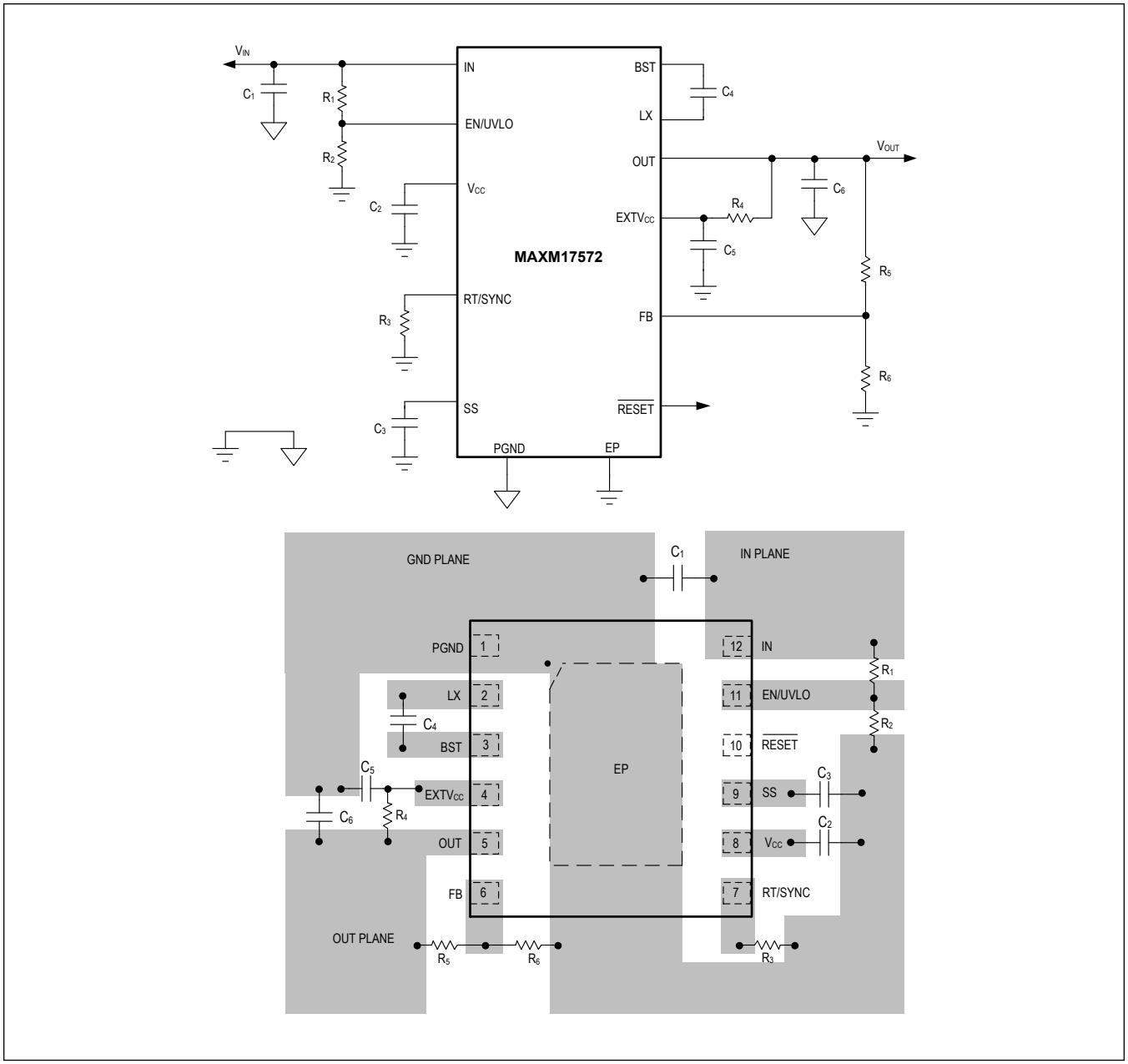
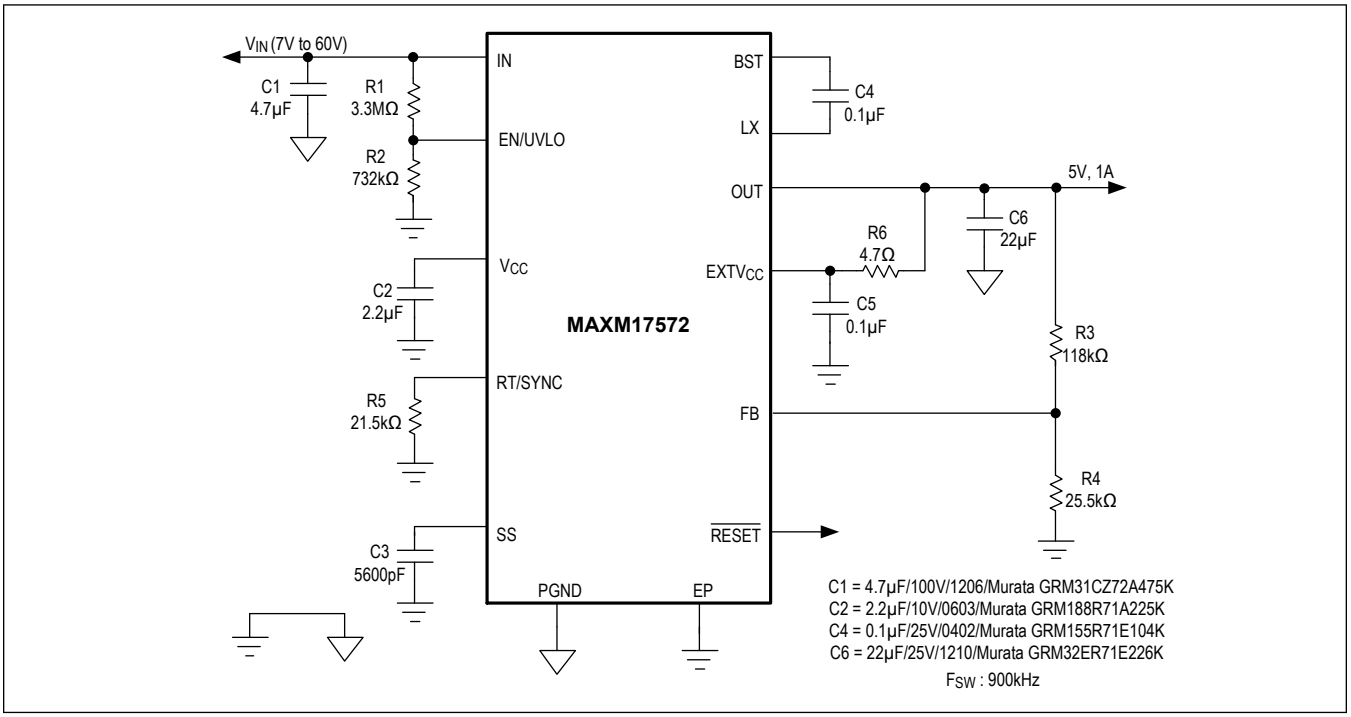


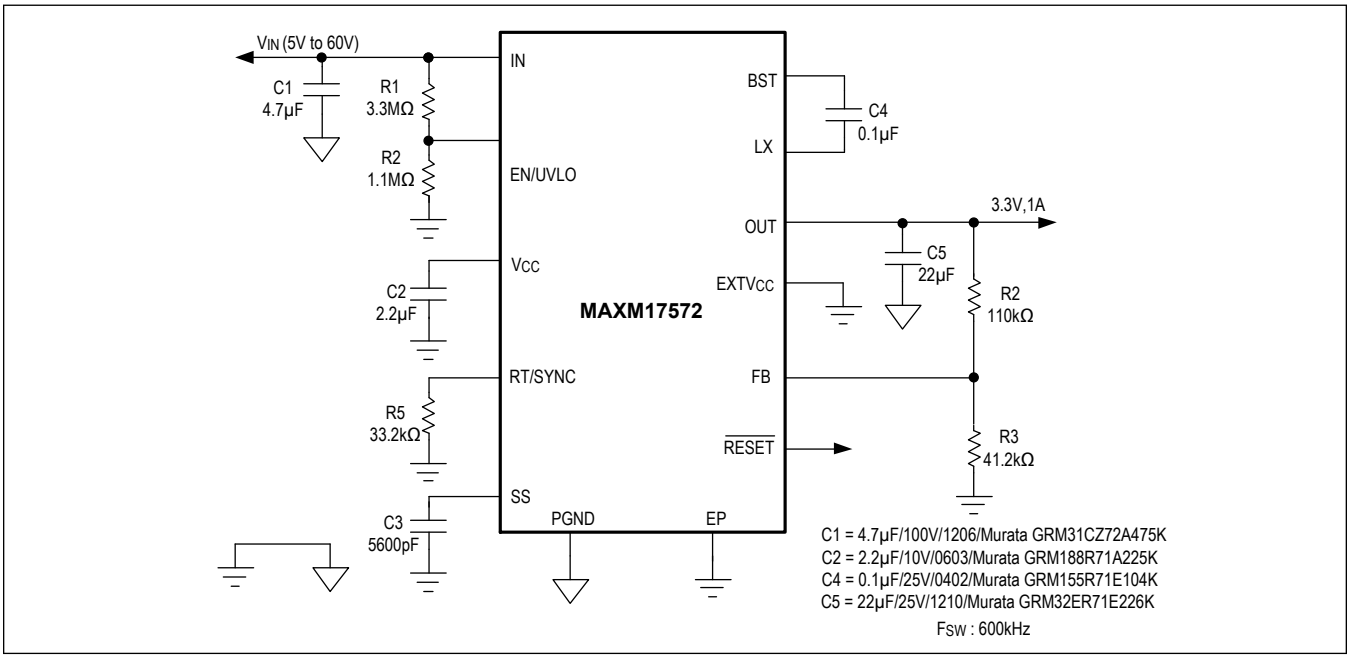
Figure 4. Layout Guidelines

Typical Application Circuits

5V Output Typical Application Circuit



3.3V Output Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN PACKAGE
MAXM17572AMC+	-40°C to +125°C	12-pin 3.5mm x 3.5mm x 2.3mm uSLIC Package
MAXM17572AMC+T	-40°C to +125°C	12-pin 3.5mm x 3.5mm x 2.3mm uSLIC Package

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/21	Release for Market Intro	—