

International
IR Rectifier

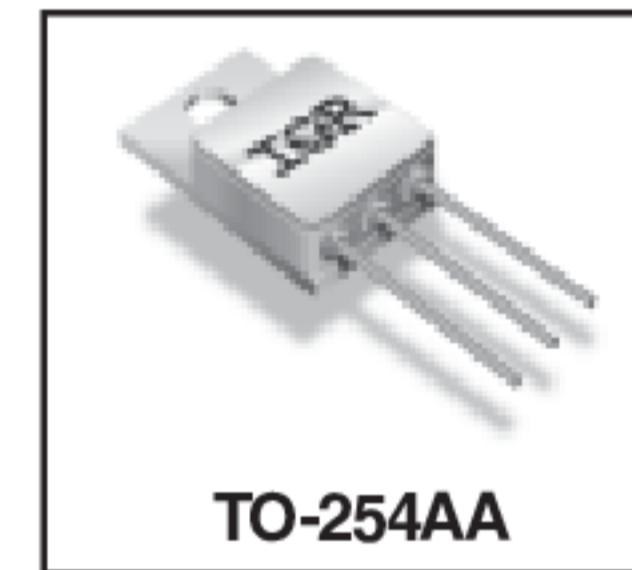
POWER MOSFET THRU-HOLE (TO-254AA)

Product Summary

Part Number	R _{Ds(on)}	I _D
IRFM250	0.100 Ω	27.4A

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

PD-90554F
IRFM250
JANTX2N7225
JANTXV2N7225
REF:MIL-PRF-19500/592
200V, N-CHANNEL
HEXFET® MOSFET TECHNOLOGY



TO-254AA

Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light-weight

Absolute Maximum Ratings

	Parameter	Units
I _D @ V _{GS} = 10V, T _C = 25°C	Continuous Drain Current	27.4
I _D @ V _{GS} = 10V, T _C = 100°C	Continuous Drain Current	17
I _{DM}	Pulsed Drain Current ①	110
P _D @ T _C = 25°C	Max. Power Dissipation	150
	Linear Derating Factor	1.2
V _{GS}	Gate-to-Source Voltage	±20
E _{AS}	Single Pulse Avalanche Energy ②	500
I _{AR}	Avalanche Current ①	27.4
E _{AR}	Repetitive Avalanche Energy ①	15
dv/dt	Peak Diode Recovery dv/dt ③	5.0
T _J	Operating Junction	-55 to 150
T _{STG}	Storage Temperature Range	°C
	Lead Temperature	300 (0.063 in.(1.6mm) from case for 10s)
	Weight	9.3 (Typical)
		g

For footnotes refer to the last page

Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0\text{V}, I_D = 1.0\text{mA}$
$\Delta BVDSS/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.28	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.100	Ω	$V_{GS} = 10\text{V}, I_D = 17\text{A}$ ^④
		—	—	0.105		$V_{GS} = 10\text{V}, I_D = 27.4\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	9.0	—	—	S	$V_{DS} = 15\text{V}, I_{DS} = 17\text{A}$ ^④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 160\text{V}, V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 160\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20\text{V}$
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20\text{V}$
Q_g	Total Gate Charge	—	—	115	nC	$V_{GS} = 10\text{V}, I_D = 27.4\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	22		$V_{DS} = 100\text{V}$
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	60		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	$V_{DD} = 100\text{V}, I_D = 27.4\text{A}, V_{GS} = 10\text{V}, R_G = 2.35\Omega$
t_r	Rise Time	—	—	190		
$t_{d(off)}$	Turn-Off Delay Time	—	—	170		
t_f	Fall Time	—	—	130		
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	3500	—	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	700	—		
C_{rss}	Reverse Transfer Capacitance	—	110	—		
C_{DC}	Drain-to-Case Capacitance	—	12	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	27.4	A	
I_{SM}	Pulse Source Current (Body Diode) ^①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.9	V	$T_j = 25^\circ\text{C}, I_S = 27.4\text{A}, V_{GS} = 0\text{V}$ ^④
t_{rr}	Reverse Recovery Time	—	—	950	ns	$T_j = 25^\circ\text{C}, I_F = 27.4\text{A}, di/dt \leq 100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovery Charge	—	—	9.0		$V_{DD} \leq 50\text{V}$ ^④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.83	$^\circ\text{C}/\text{W}$	
R_{thJCS}	Case-to-Sink	—	0.21	—		
R_{thJA}	Junction-to-Ambient	—	—	48		Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier website.

For footnotes refer to the last page

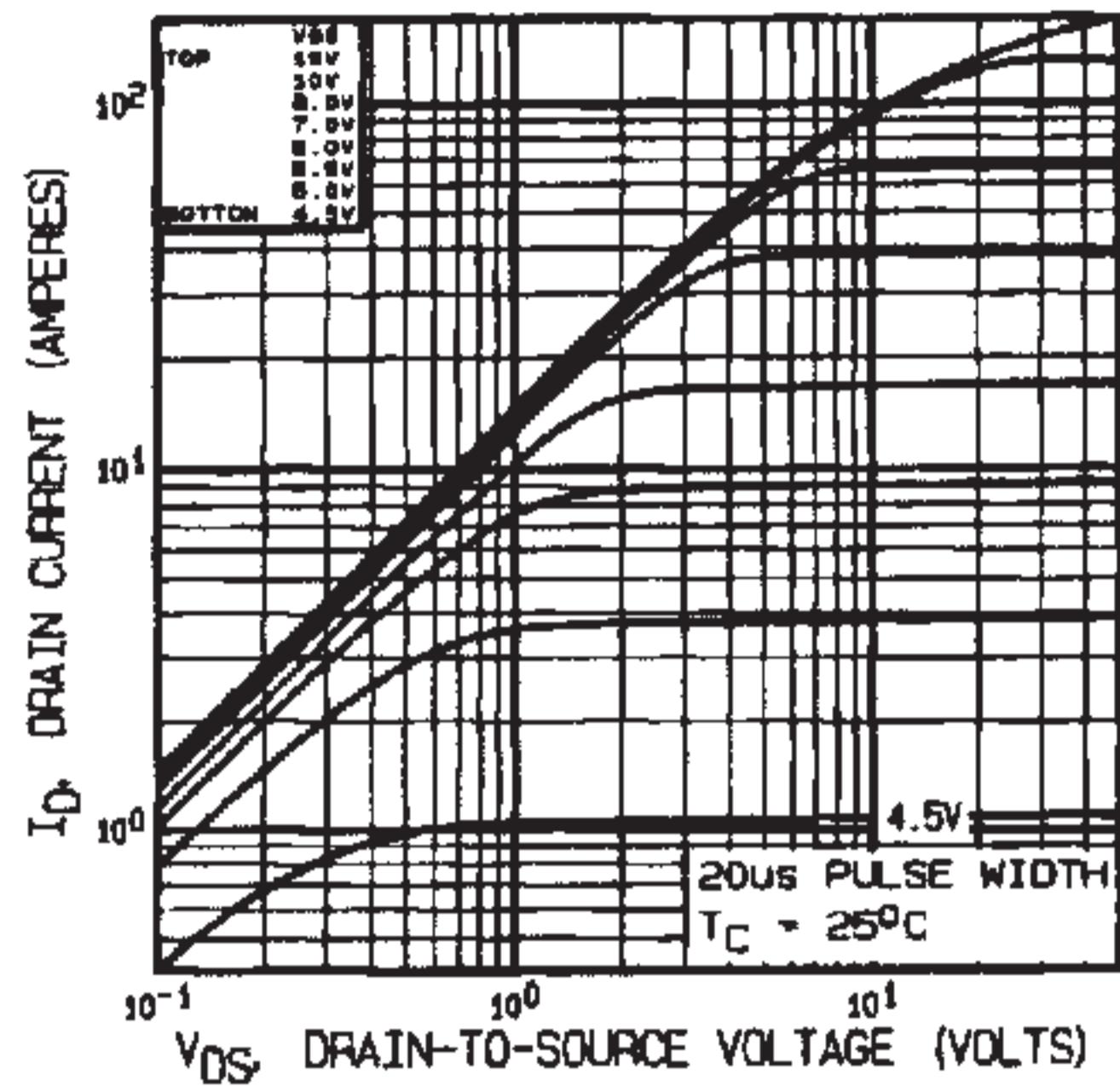


Fig 1. Typical Output Characteristics

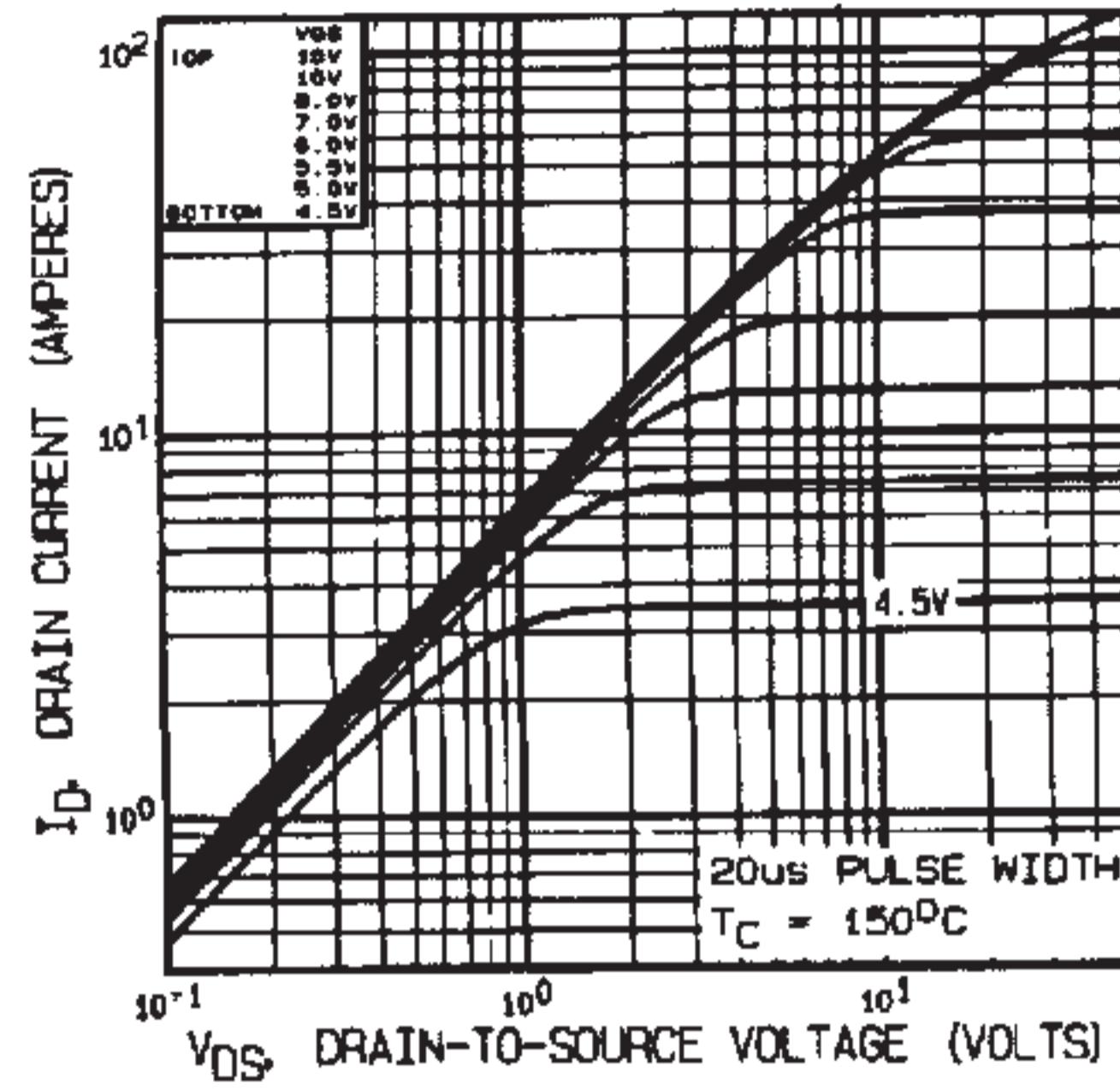


Fig 2. Typical Output Characteristics

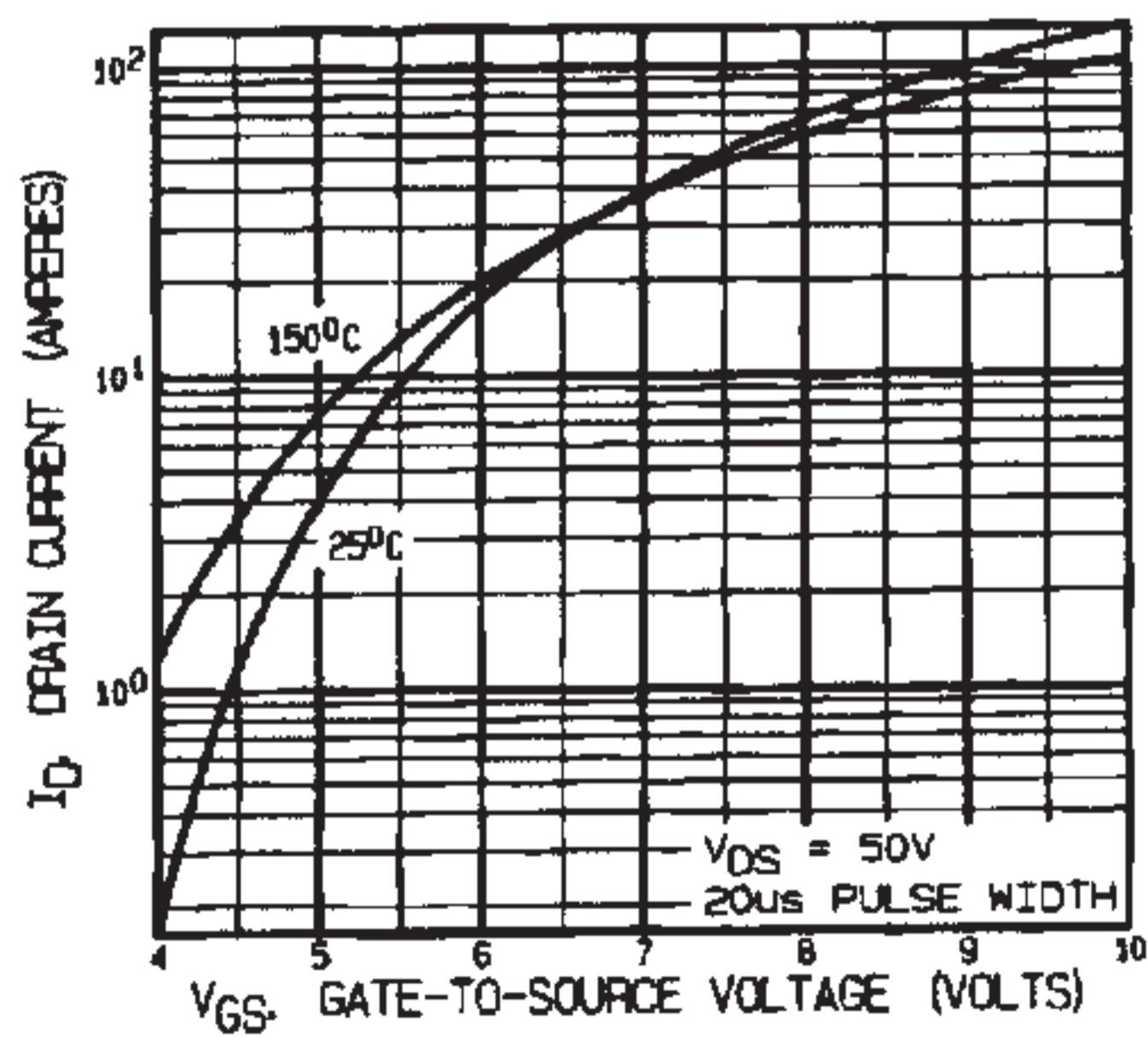


Fig 3. Typical Transfer Characteristics

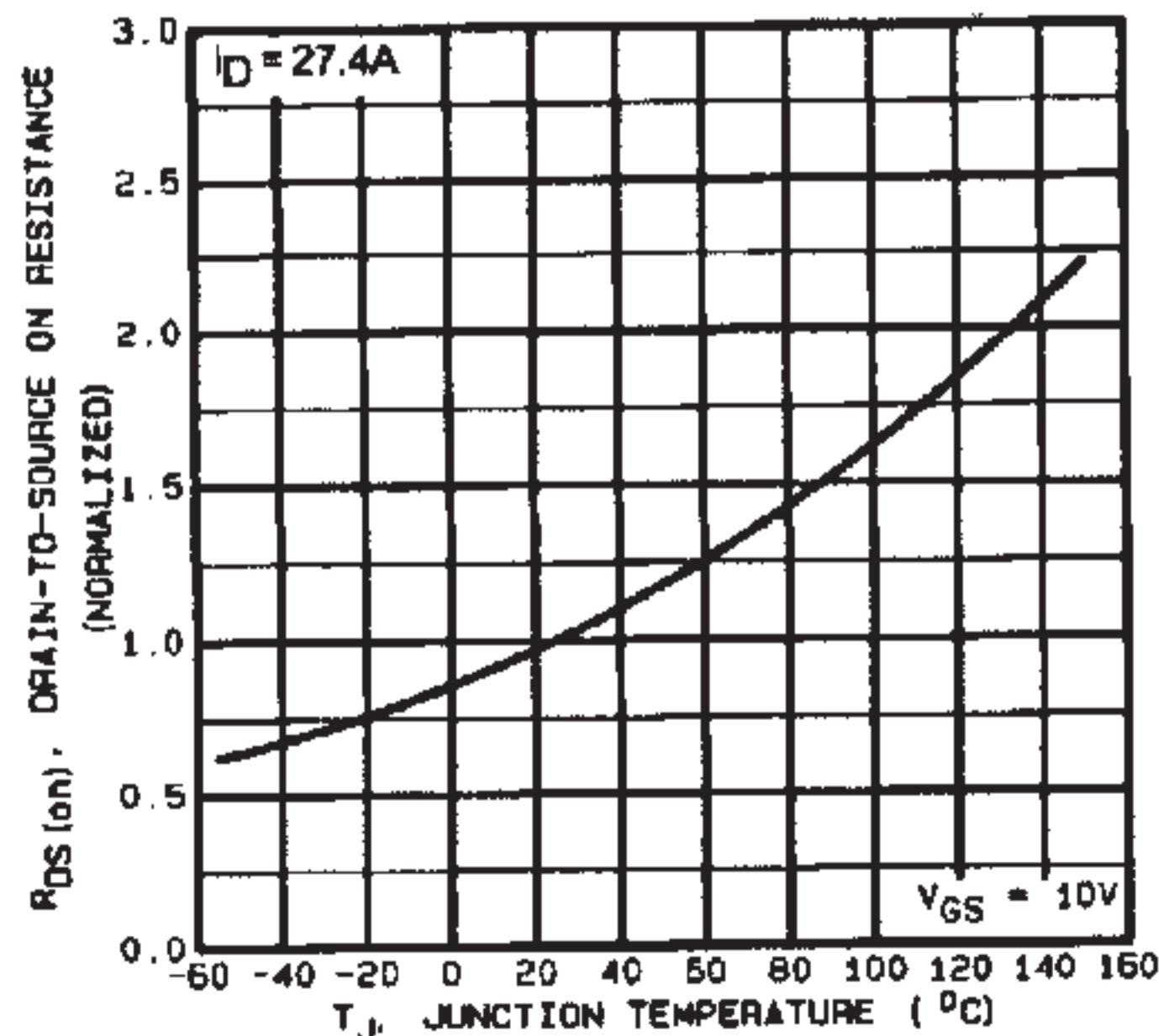


Fig 4. Normalized On-Resistance
Vs. Temperature

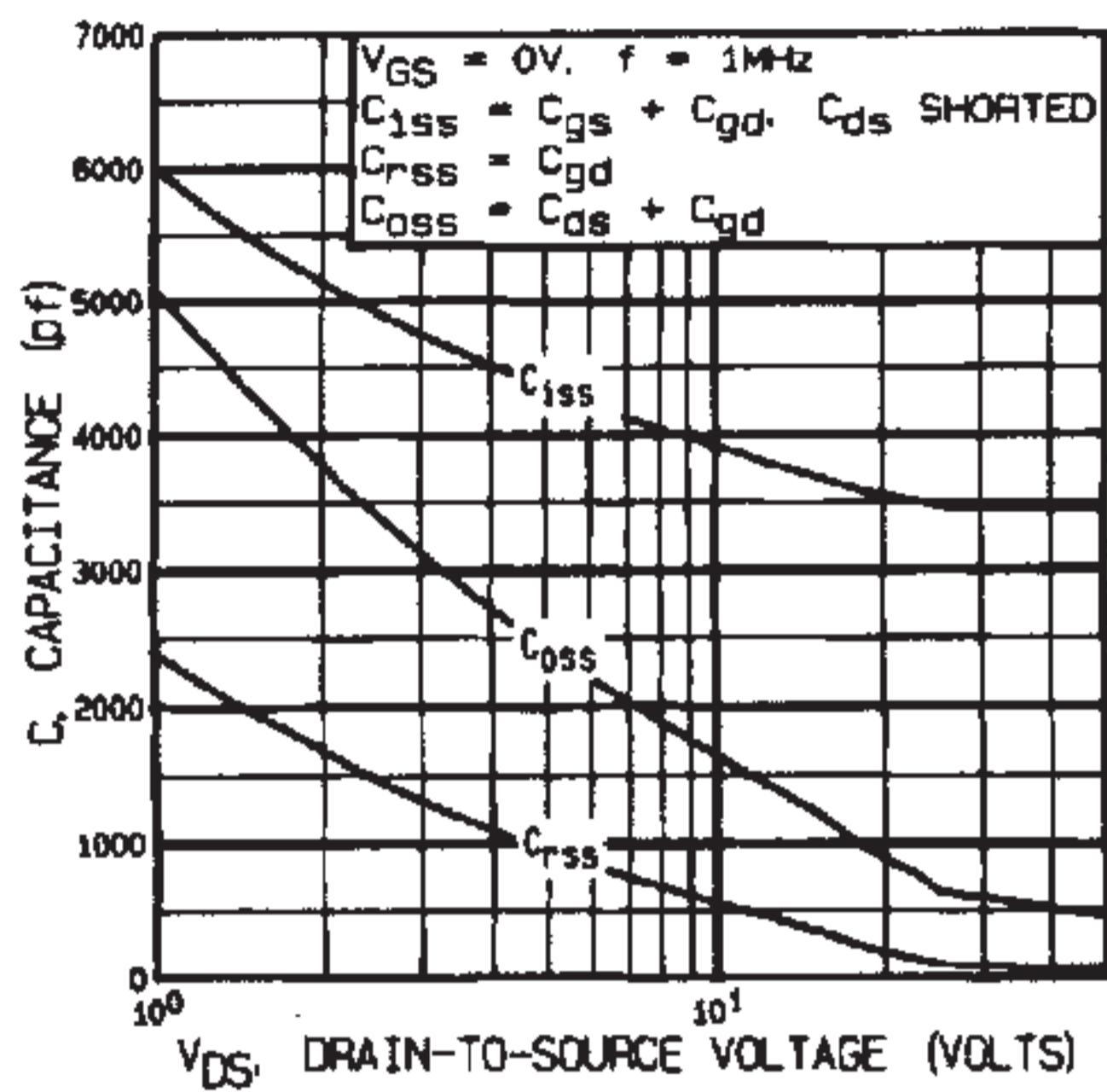


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

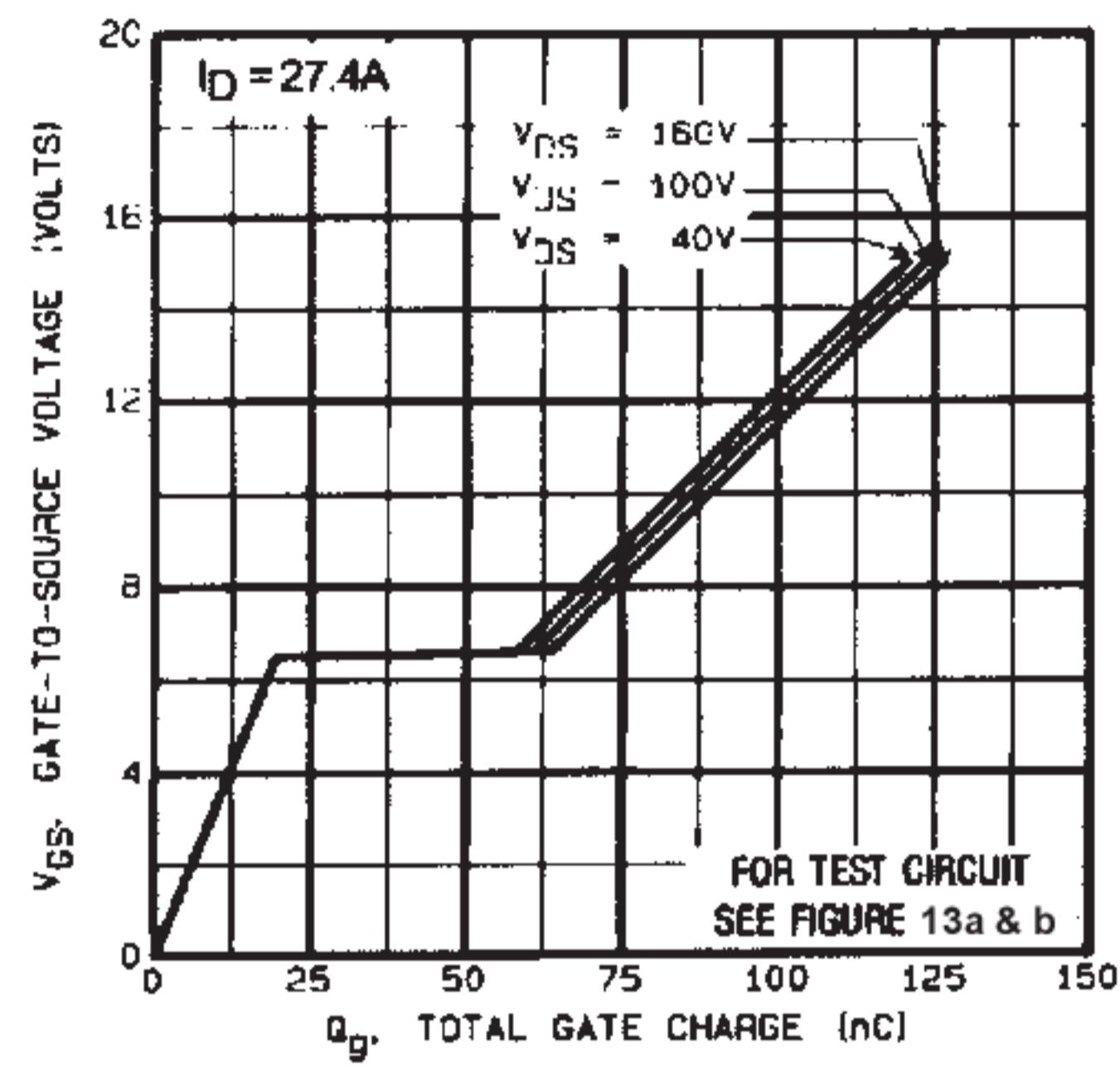


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

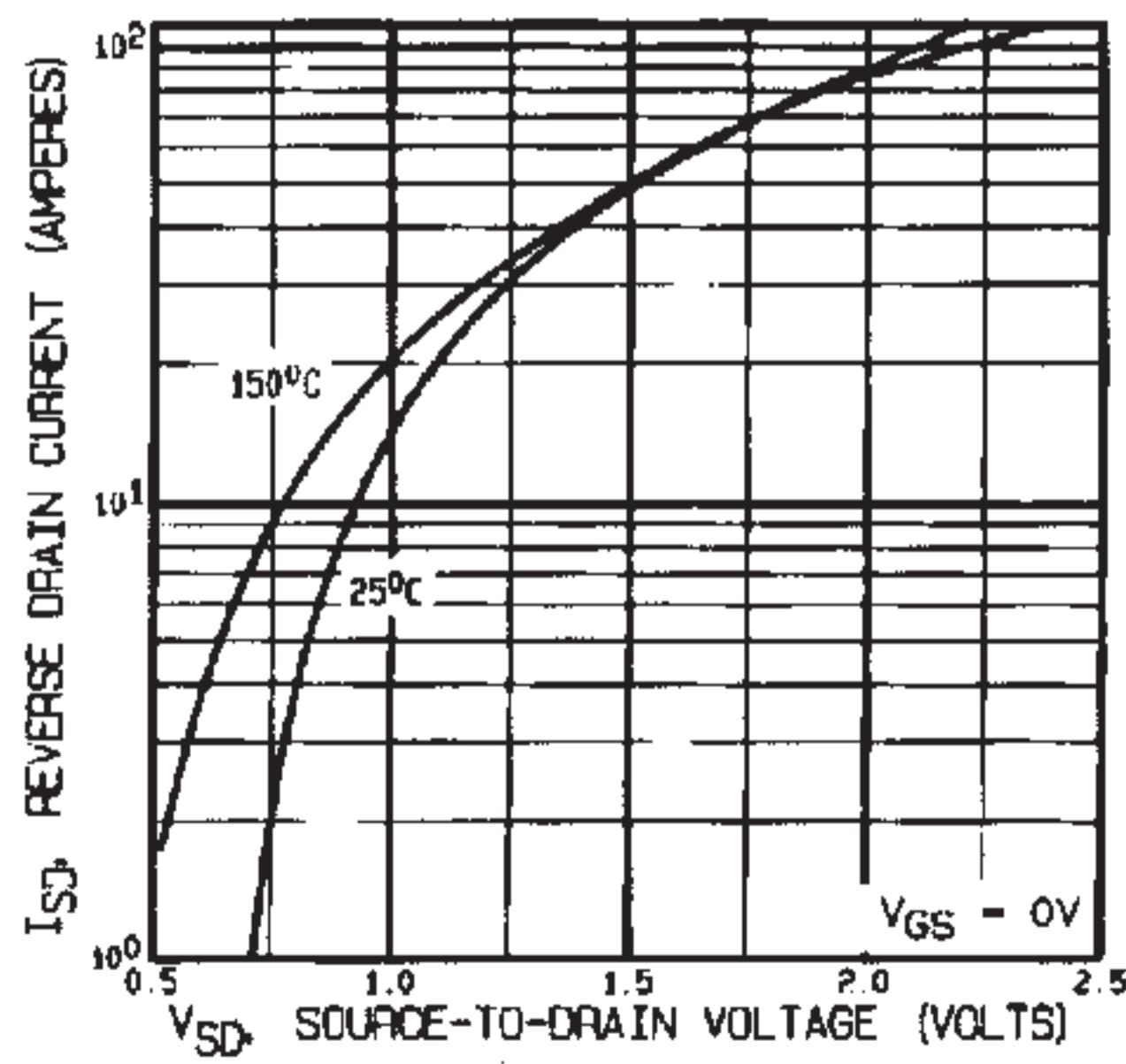


Fig 7. Typical Source-Drain Diode
Forward Voltage

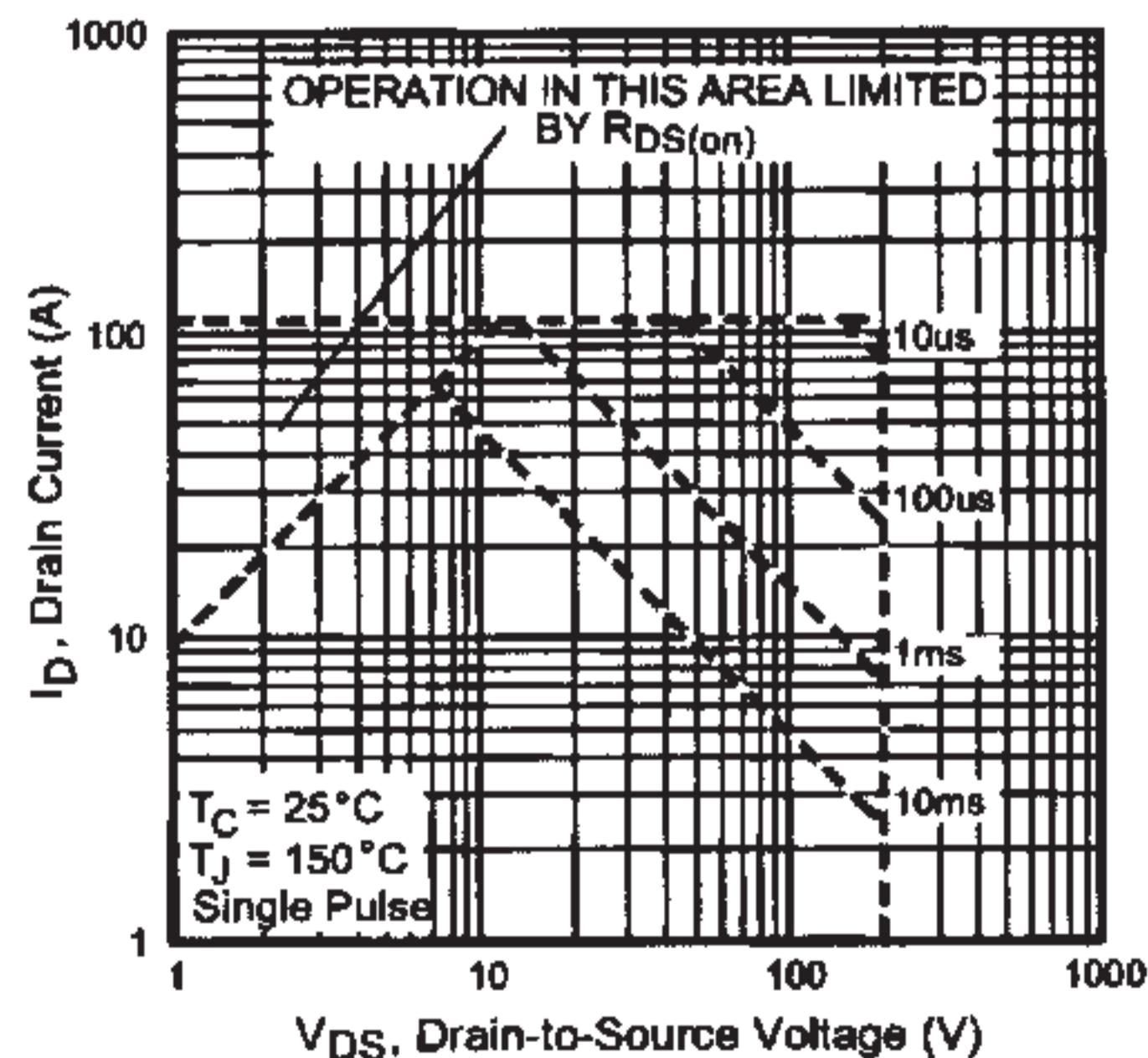


Fig 8. Maximum Safe Operating Area

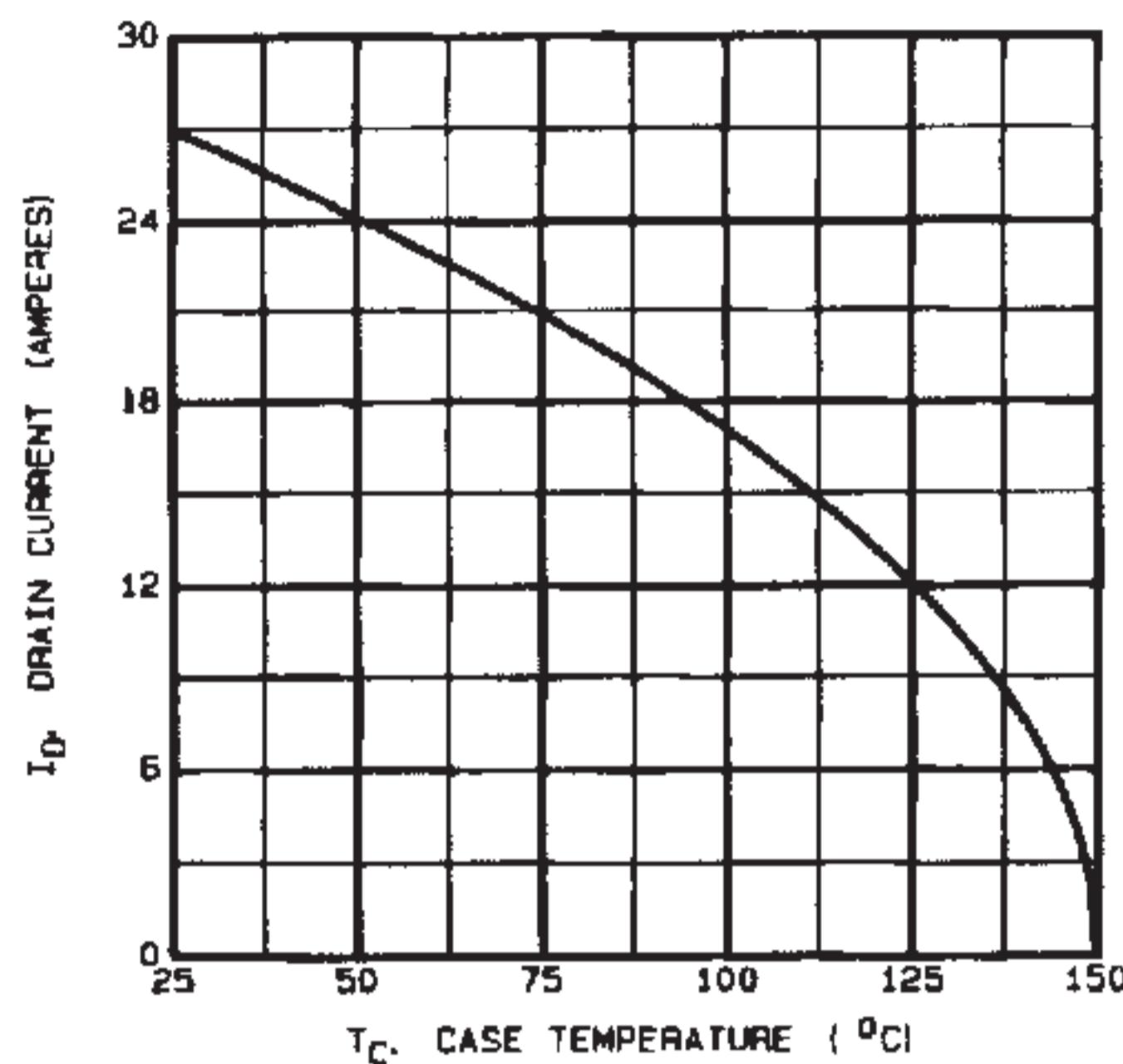


Fig 9. Maximum Drain Current Vs.
Case Temperature

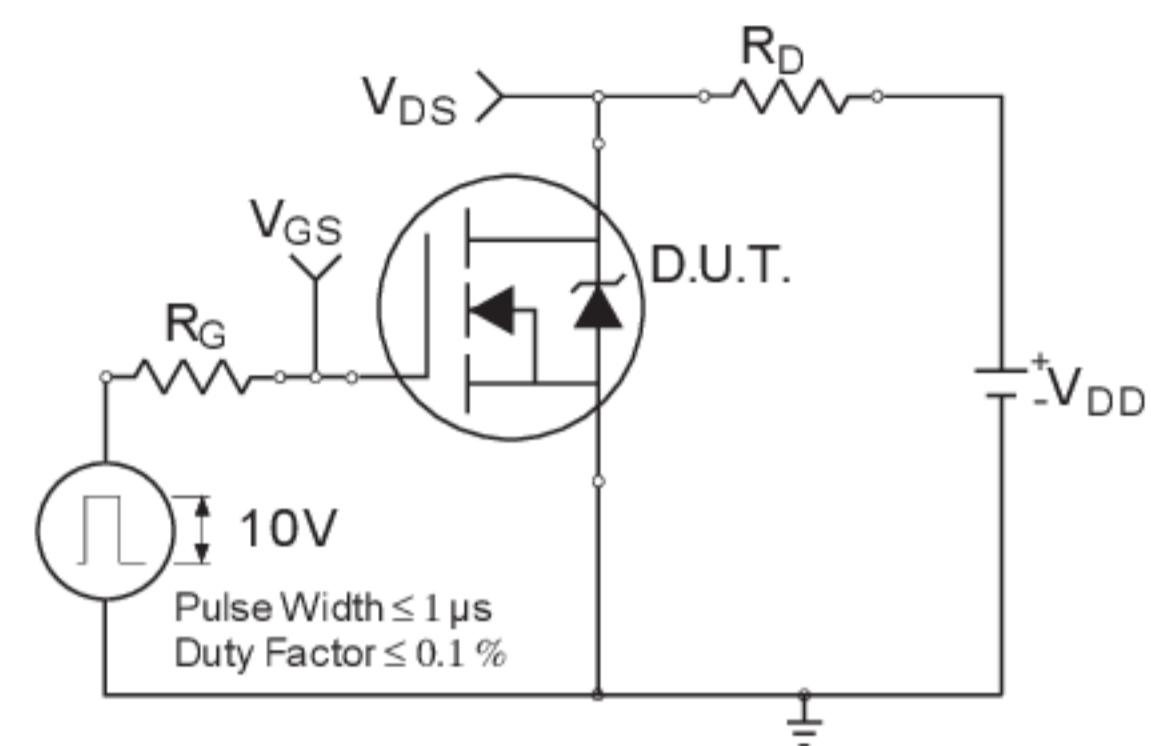


Fig 10a. Switching Time Test Circuit

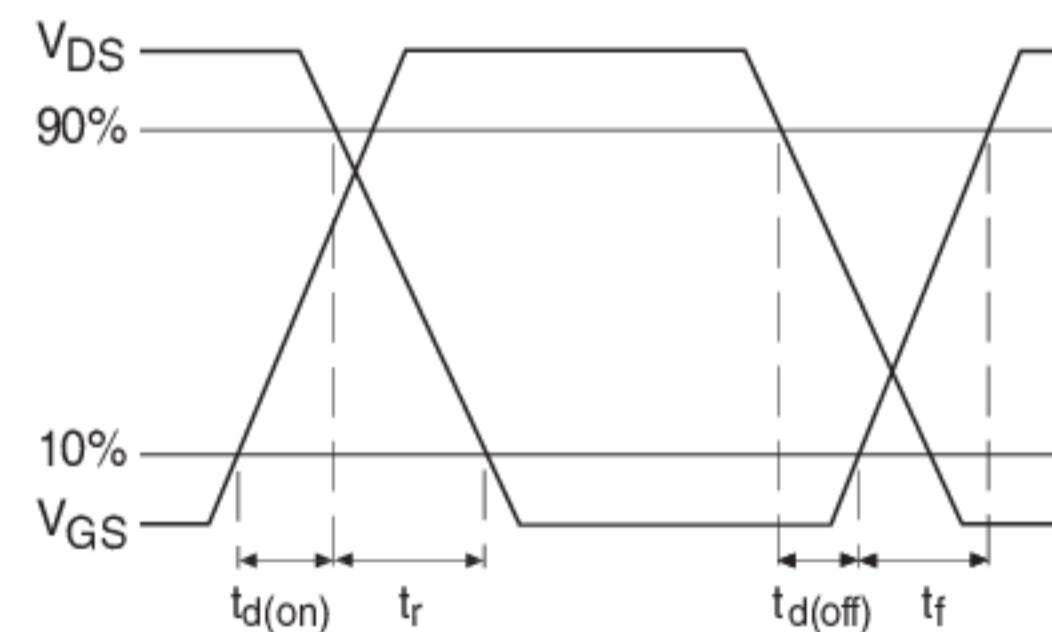


Fig 10b. Switching Time Waveforms

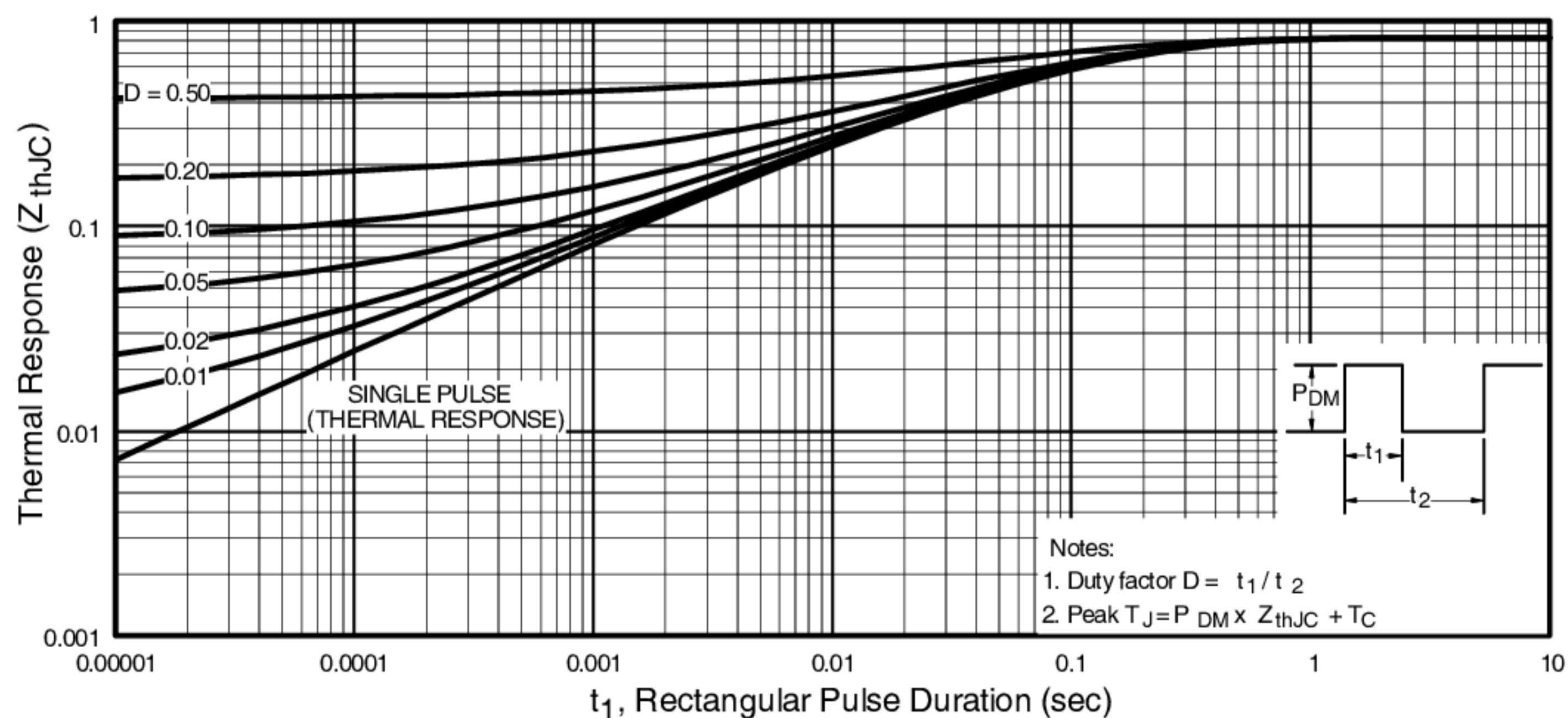
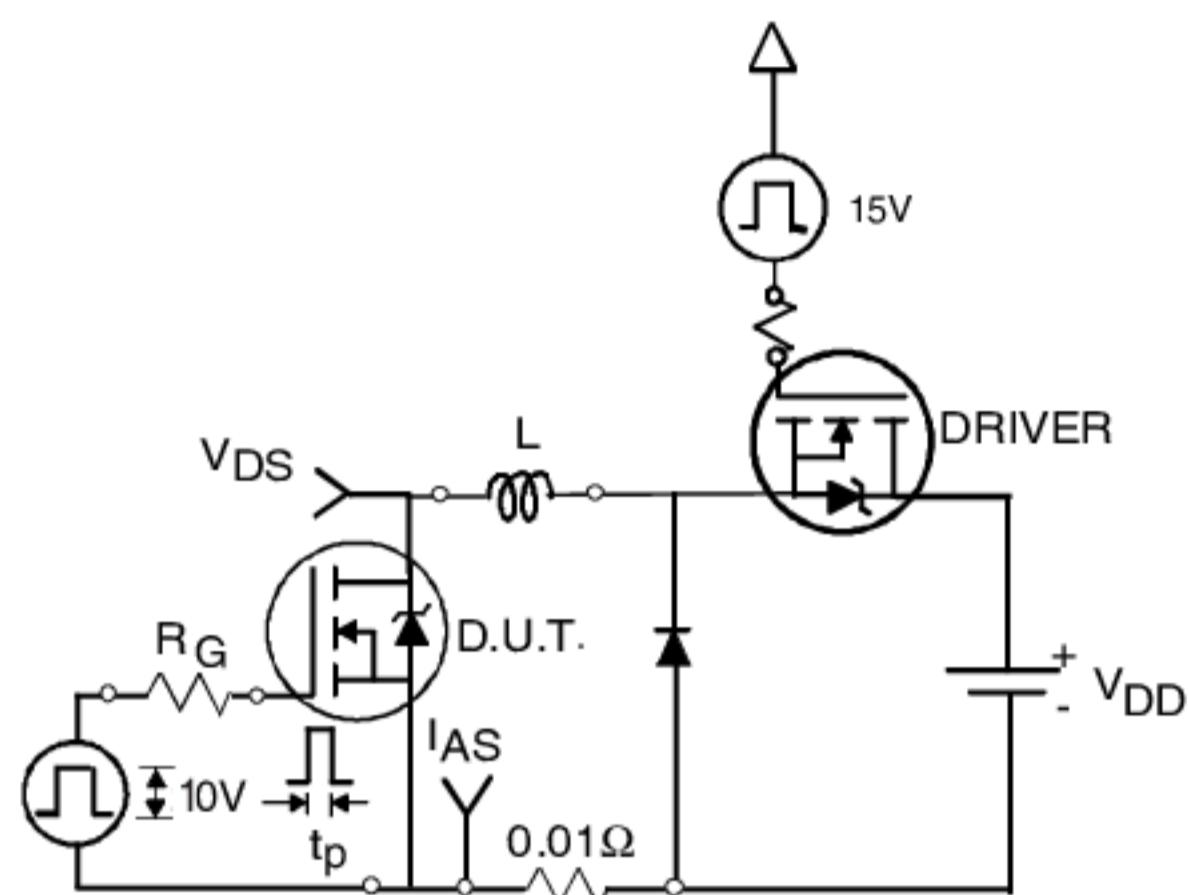
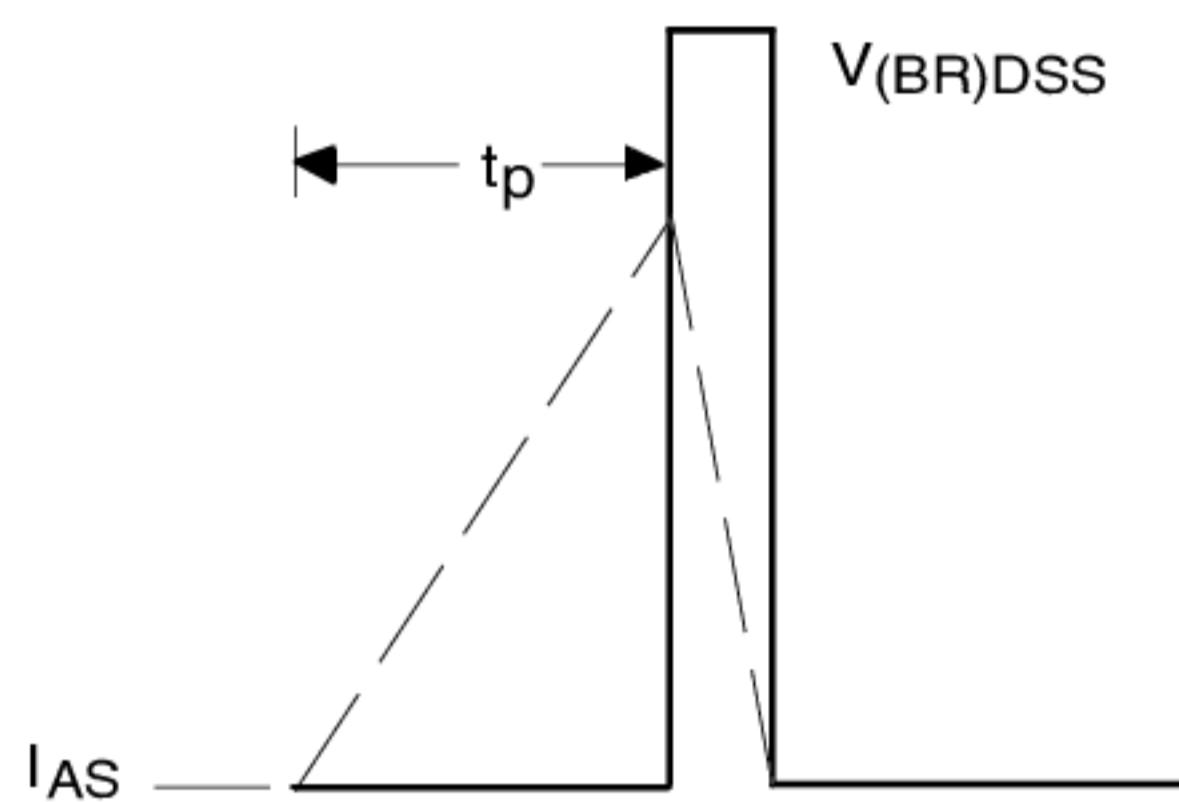
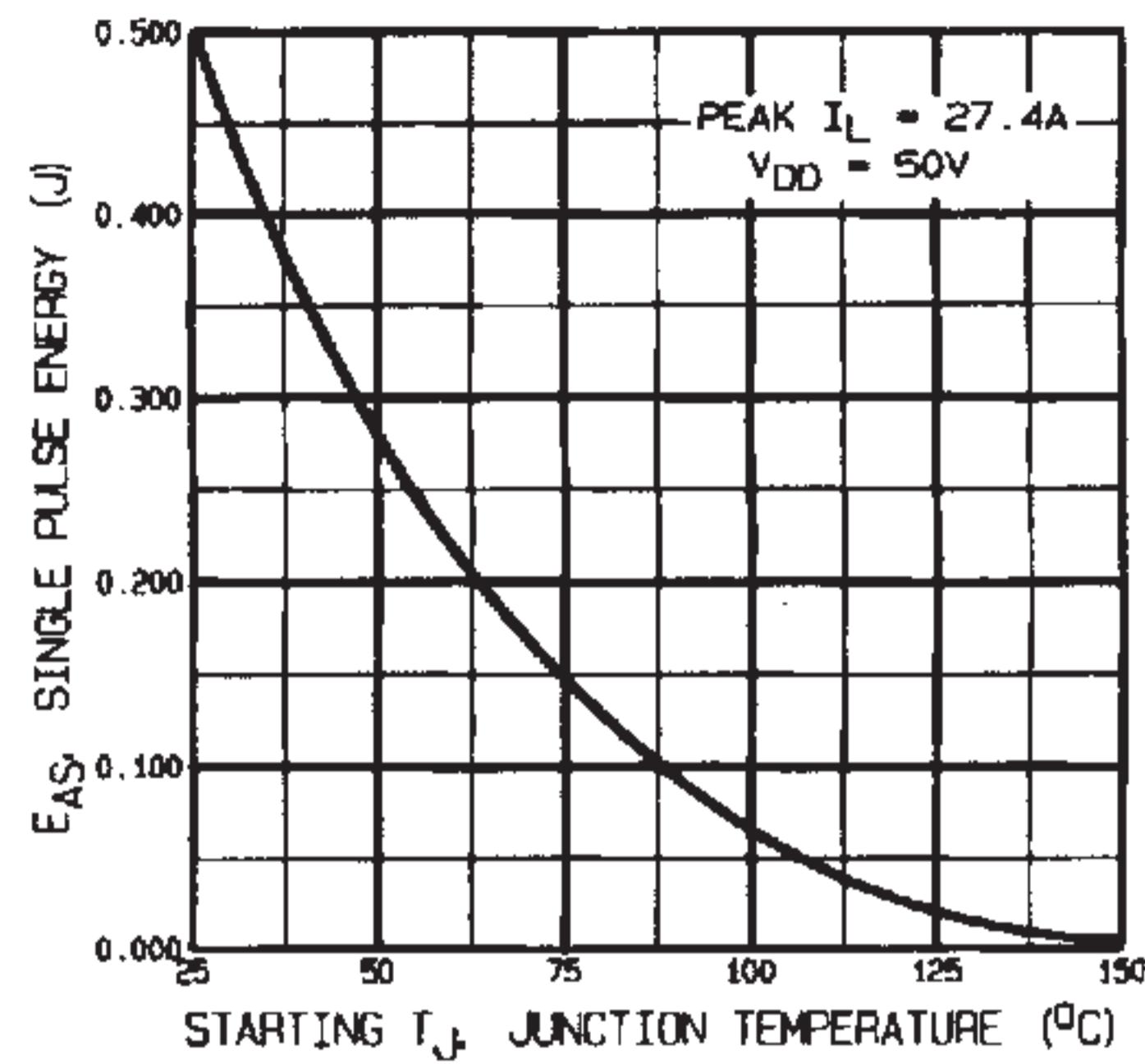
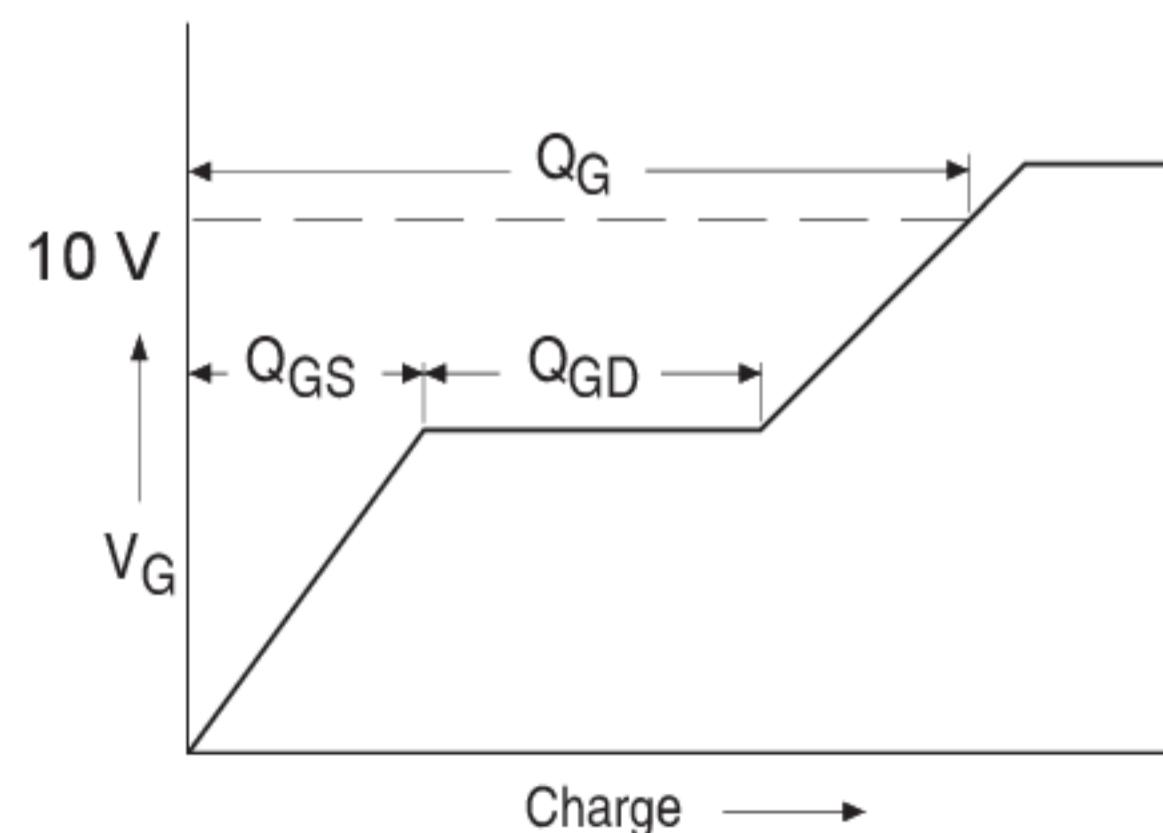
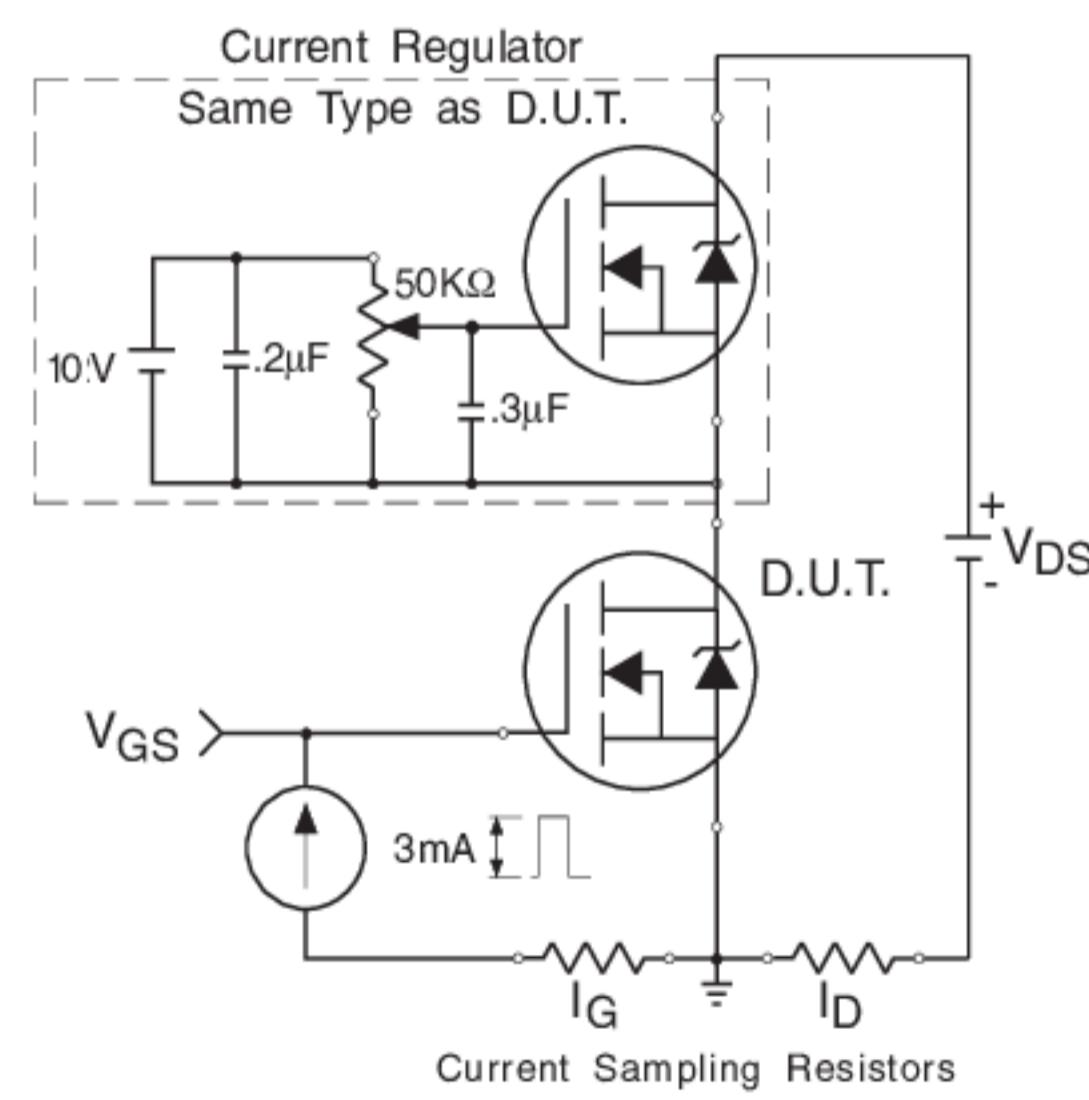


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

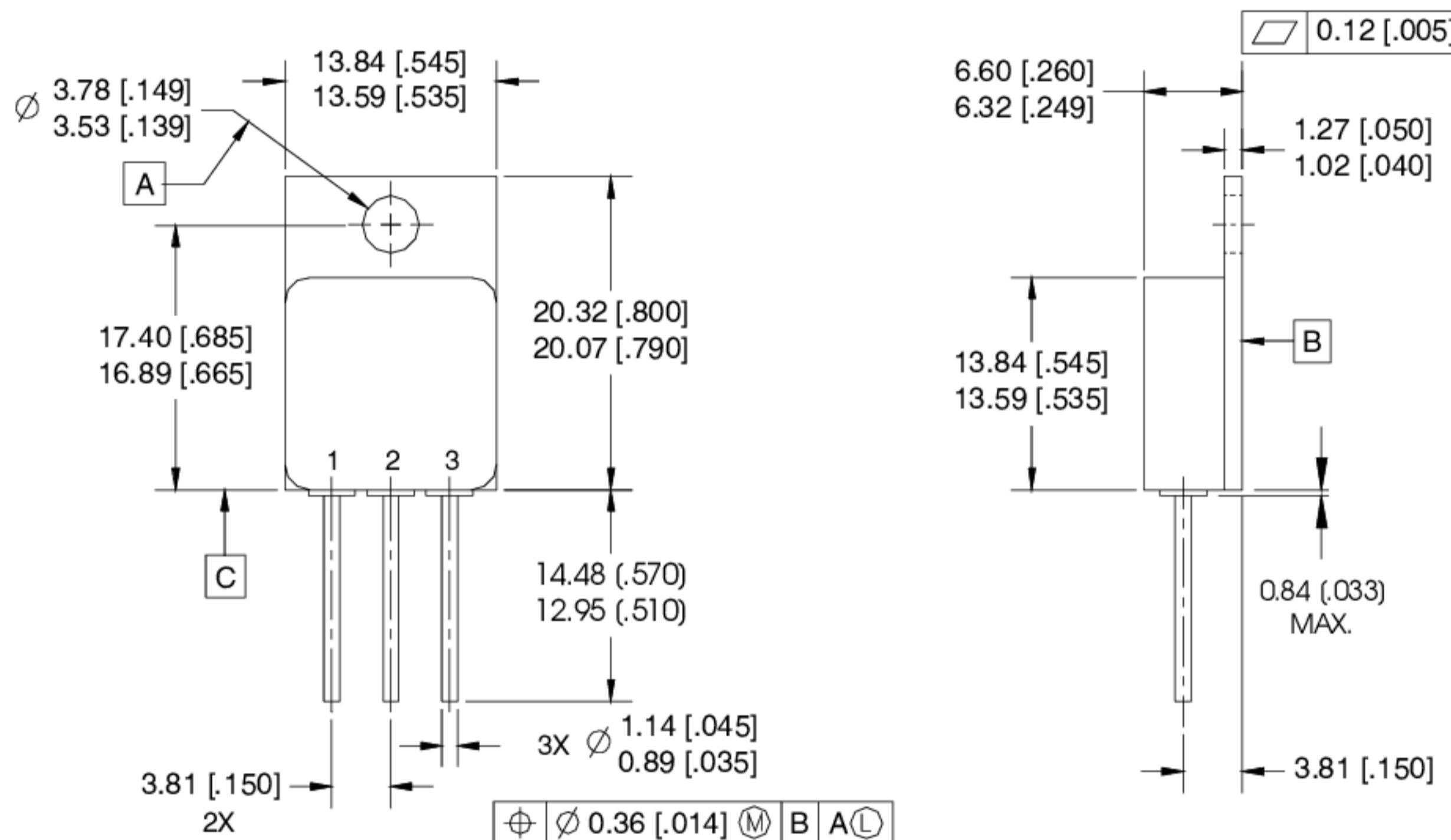
**Fig 12a.** Unclamped Inductive Test Circuit**Fig 12b.** Unclamped Inductive Waveforms**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current**Fig 13a.** Basic Gate Charge Waveform**Fig 13b.** Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 1.3mH$
Peak $I_L = 27.4A$, $V_{GS} = 10V$

- ③ $I_{SD} \leq 27.4A$, $di/dt \leq 190A/\mu s$,
 $V_{DD} \leq 200V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

CAUTION

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

International
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Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 10/2011