

12V P-Channel Enhancement Mode MOSFET

Description

The NP1207DR uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

General Features

- ◆ $V_{DS} = -12V$, $I_D = -7A$
 $R_{DS(ON)}(Typ.) = 25m\Omega$ @ $V_{GS} = -4.5V$
 $R_{DS(ON)}(Typ.) = 34m\Omega$ @ $V_{GS} = -2.5V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

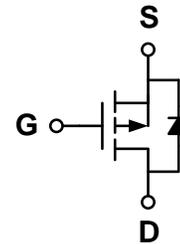
Application

- ◆ PWM applications
- ◆ Load switch

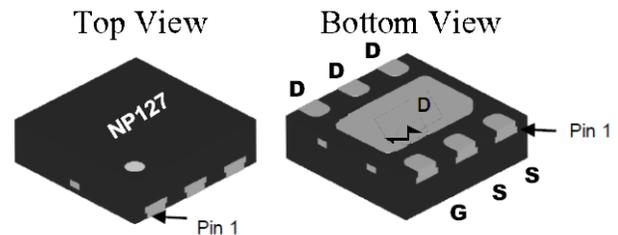
Package

- ◆ DFN2*2-6L

Schematic diagram



Marking and pin assignment



NP----Natlinear Power
 127-----NP1207



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP1207DR-G	-55°C to +150°C	DFN2*2-6L	4000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	-12	V
Gate-source voltage	V_{GS}	±12	V
Drain current-continuous ^a @ $T_j = 125^\circ C$ -pulse ^b	I_D	-7	A
	I_{DM}	-28	A
Drain-source Diode forward current	I_S	-7	A
Maximum power dissipation	P_D	18	W
Operating junction Temperature range	T_j	-55—150	°C

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-12	-16.5	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-12V, V_{GS}=0V$	-	-	-1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	± 100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.7	-1.2	V
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-7A$	-	25	35	m Ω
		$V_{GS}=-2.5V, I_D=-6A$	-	34	45	
Forward transconductance	gfs	$V_{GS}=-5V, I_D=-7A$	-	5	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	$V_{DS}=-6V, V_{GS}=0V$ $f=1.0MHz$	-	740	-	pF
Output capacitance	C_{OSS}		-	290	-	
Reverse transfer capacitance	C_{RSS}		-	190	-	
Switching Characteristics						
Turn-on delay time	$t_{D(on)}$	$V_{DD}=-6V$ $I_D=-7A$ $V_{GEN}=-4.5V$ $R_L=1.0\Omega, 2ohm$ $R_{GEN}=1ohm$	-	12.5	-	ns
Rise time	t_r		-	35	-	
Turn-off delay time	$t_{D(off)}$		-	30	-	
Fall time	t_f		-	10	-	
Total gate charge	Qg	$V_{DS}=-6V, I_D=-7A$ $V_{GS}=-4.5V$	-	7.8	-	nC
Gate-source charge	Qgs		-	1.2	-	
Gate-drain charge	Qgd		-	1.6	-	
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_S=-7A$	-	-0.81	-1.2	V

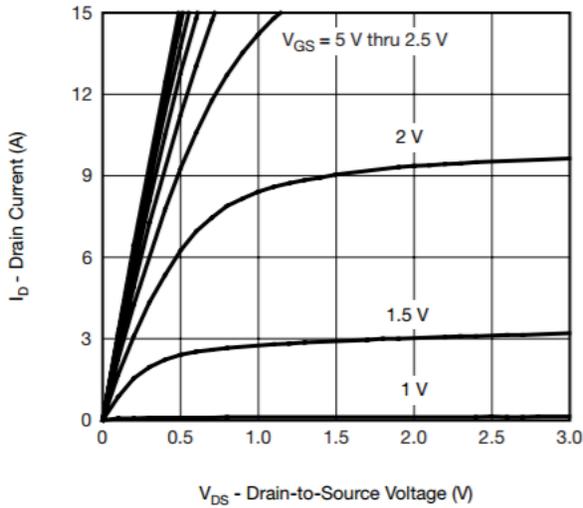
Notes:

- surface mounted on FR4 board, $t \leq 10sec$
- pulse test: pulse width $\leq 300\mu s$, duty $\leq 2\%$
- guaranteed by design, not subject to production testing

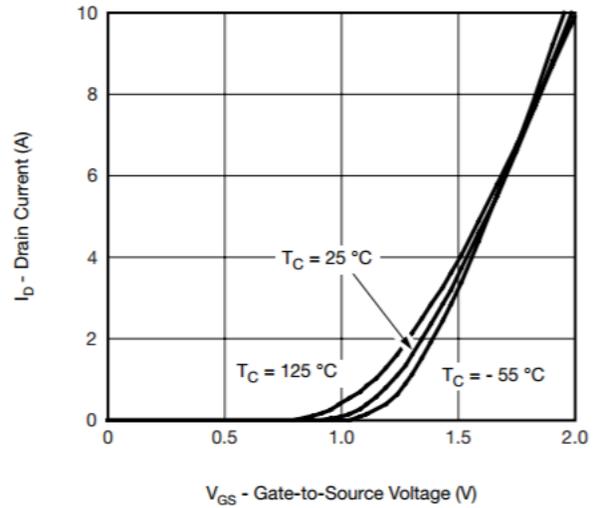
Thermal Characteristics

Thermal Resistance junction-to ambient	Rth JA	100	$^{\circ}C/W$
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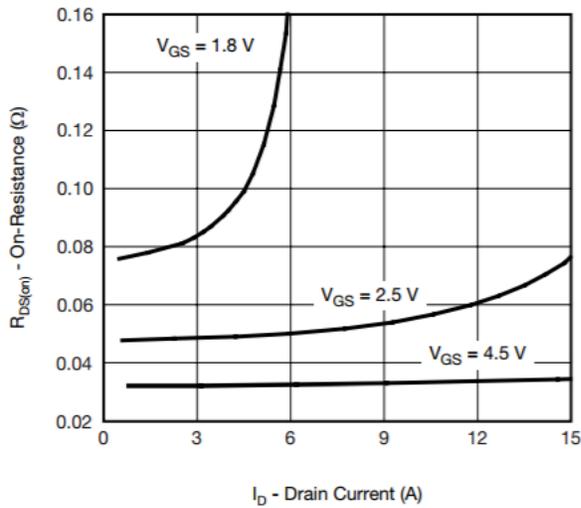
Typical Performance Characteristics



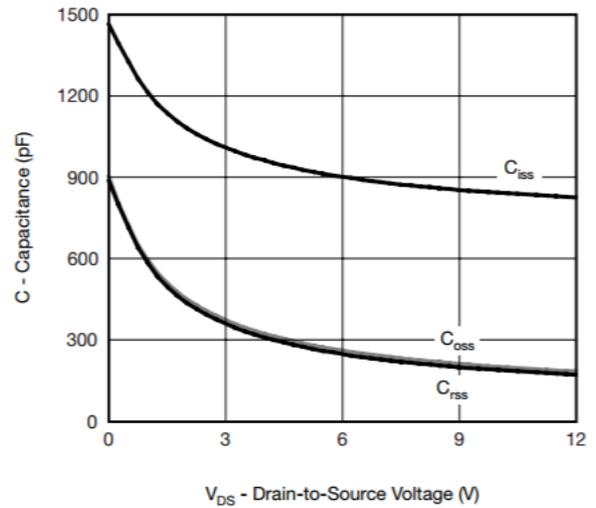
Output Characteristics



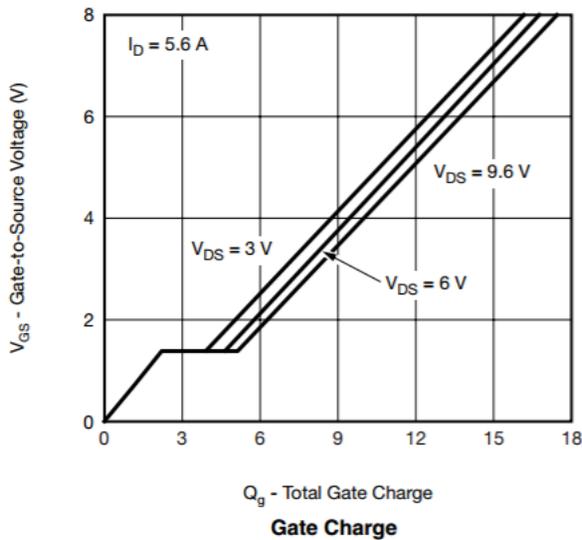
Transfer Characteristics



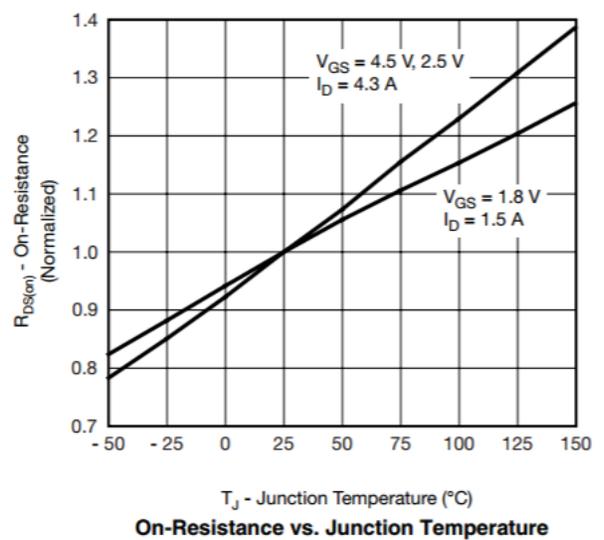
On-Resistance vs. Drain Current and Gate Voltage



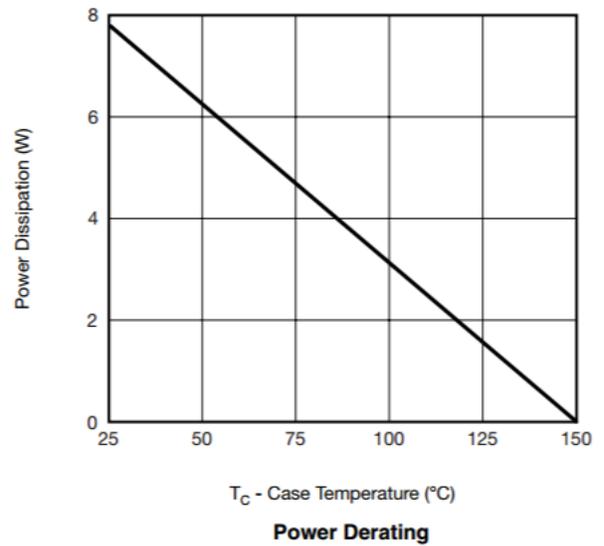
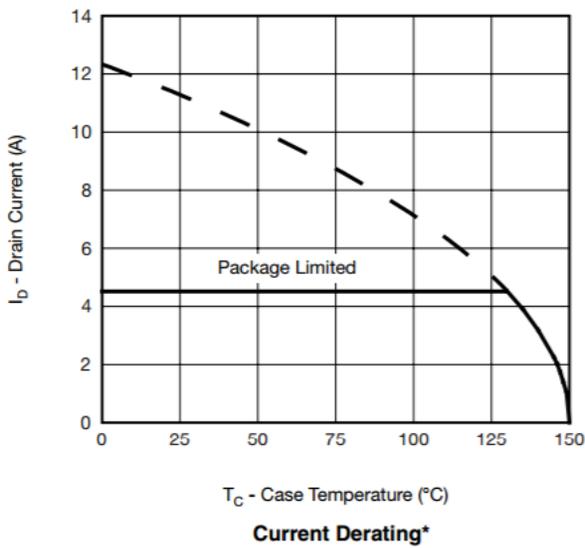
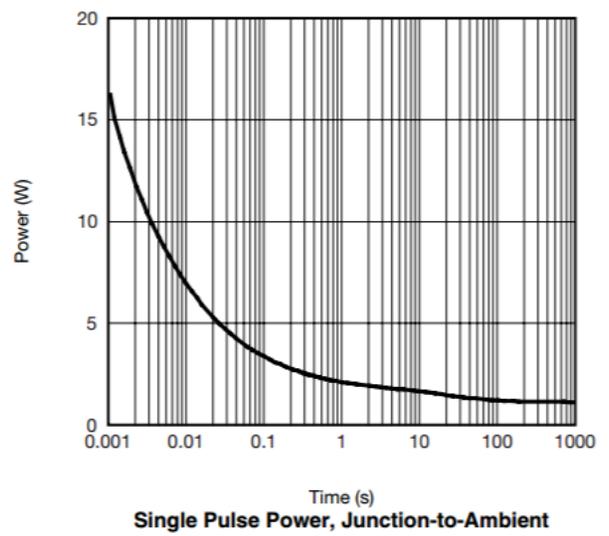
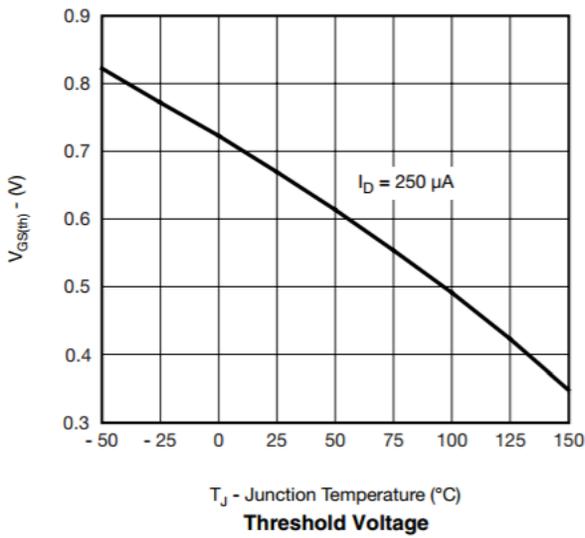
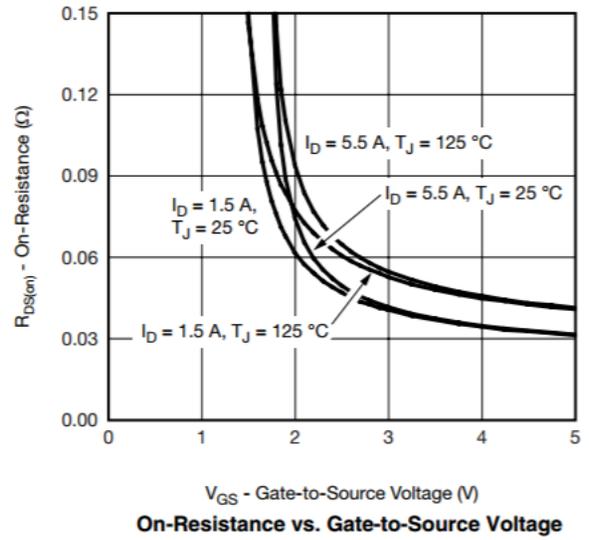
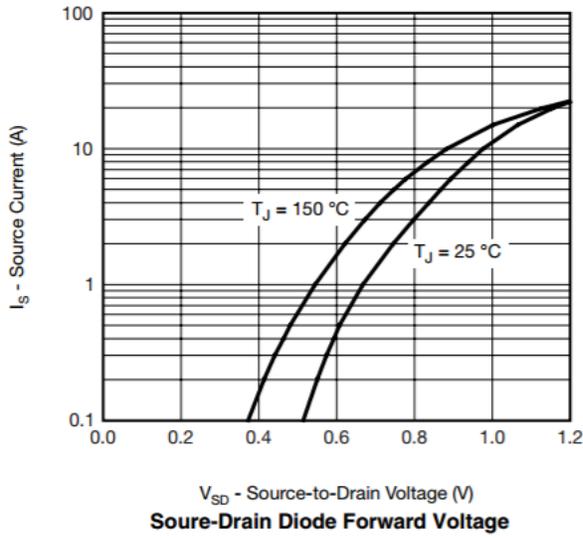
Capacitance

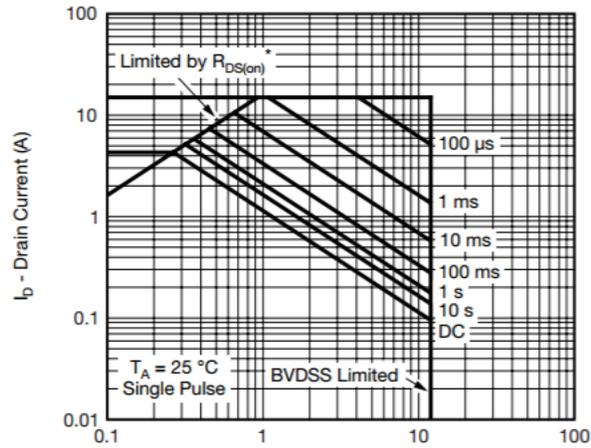


Gate Charge

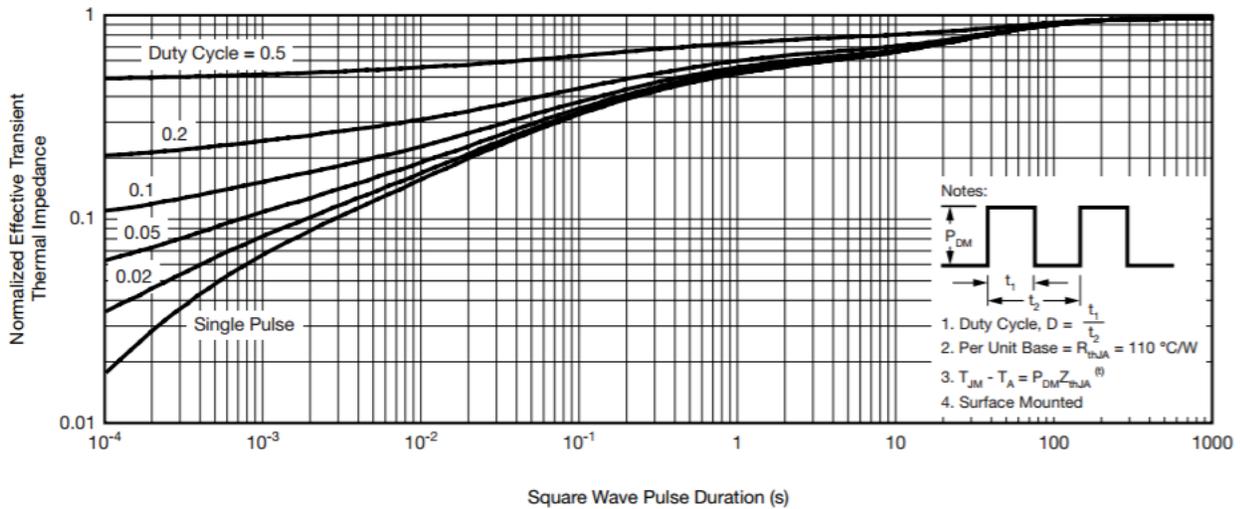


On-Resistance vs. Junction Temperature

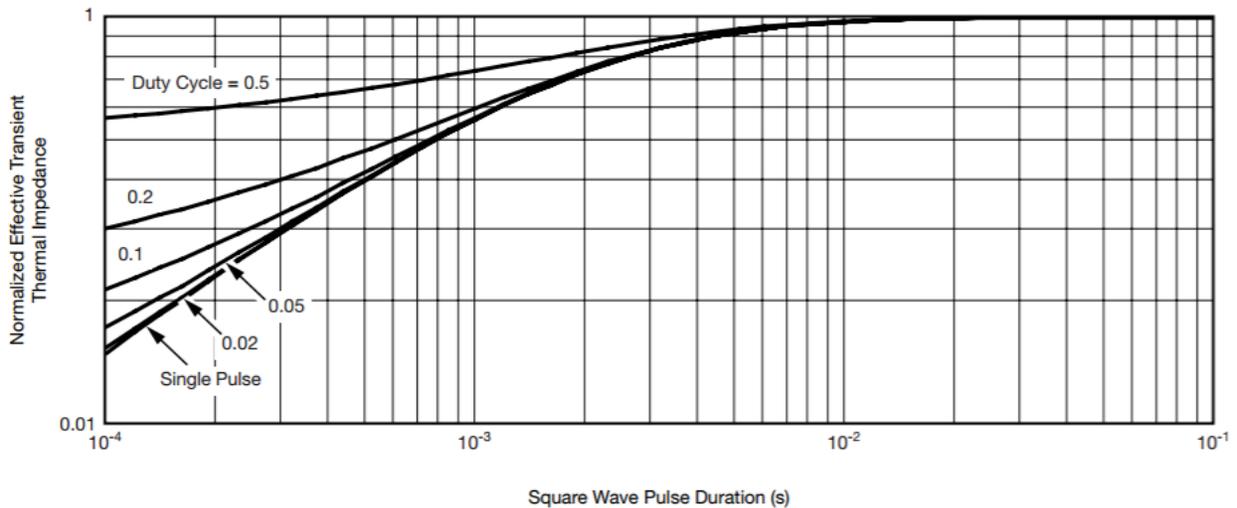




V_{DS} - Drain-to-Source Voltage (V)
 $* V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient



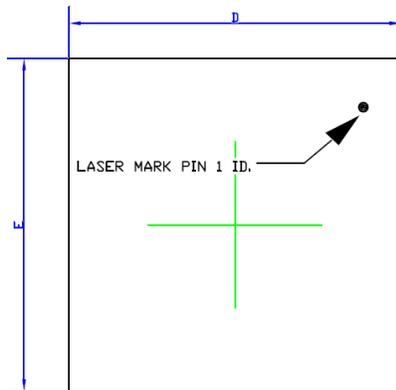
Normalized Thermal Transient Impedance, Junction-to-Ambient



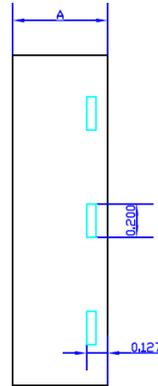
Normalized Thermal Transient Impedance, Junction-to-Case

Package Information

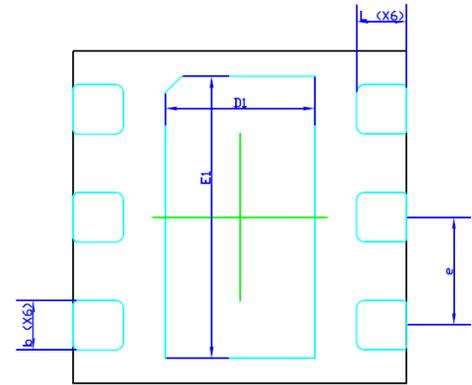
- DFN2*2-6L



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSION (MM)			
PKG	DFN2020-6L		
SYMBOL	MIN.	NOM.	MAX
A	0.527	0.552	0.577
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.80	0.90	1.00
E1	1.60	1.70	1.80
e	0.65 REF.		
L	0.25	0.30	0.35