USB Type-C PD/PPS Multi Protocol Controller

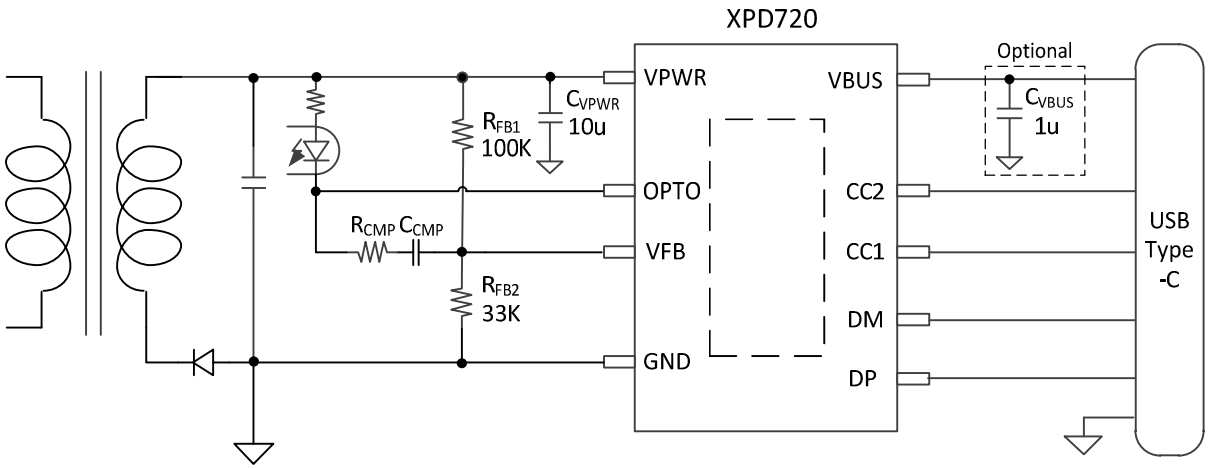
1 Features

- USB PD3.0 Certified（TID：3479）
- Support USB Type -C Protocol
  - Configure DFP（Source）
  - Broadcast 3A/1.5A Current
- Support USB Power Delivery（PD）2.0/3.0 and PPS Protocol
  - Integrated PD Layered Communication Protocol
  - Support 5V，9V and 12V PDOs
  - Output Power up to 36W
  - Support 5V Prog，9V Prog APDOs
- Integrated QC2.0/3.0/3.0+ Quick Charge Protocol
  - Support Xiao Mi CHARGE TURBO 27W Protocol
- Integrated FCP/SCP/HVSCP Fast Charging Protocol
  - Support HUAWEI 10V HVSCP Protocol
- Support AFC Fast Charging Protocol
- Support USB BC1.2 DCP
- Support Apple 2.4A
- Integrated Constant Voltage(CV) Loop Compensation
  - Integrated Secondary Side Compensation Circuit, such as TL431
- Integrated 10mΩ VBUS Path Power switch
- Integrated 10mΩ Current Sense
- Built-in VPWR and VBUS Double Discharge path
- Support Line Loos Compensation
- Multiple Protection
  - Over Voltage protection
  - Under Voltage protection
  - Over Current protection
  - Over Temperature Protection
- CC1/CC2/DP/DM Over Voltage protection
- ±4KV ESD HBM
- ESOP8 package

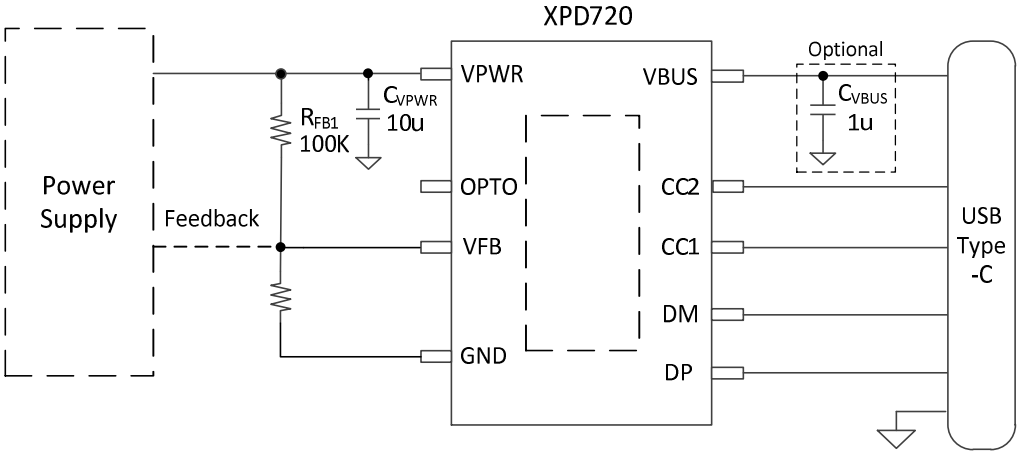
2 Applications

- AC-DC power adapter
- Car Charge
- USB-PD converter

3 Typical Application Circuit



AC-DC Application Circuit



DC-DC Application Circuit

4 General Description

The XPD720 is a high performance, high-integrated USB Type-C Power Delivery source controller. The XPD720 supports USB Type-C Power Delivery (PD) 2.0 / 3.0 and PPS, QC3.0 + / QC 3.0 / QC 2.0 fast charging protocol, Huawei FCP / SCP / HVSCP fast charging protocol, Samsung AFC fast charging protocol, BC1.2 DCP and Apple device 2.4A charging specification. It provides a cost-effective USB Type-C port charging solution for AC-DC adapter, car charger and other devices.

The built-in Type-C protocol of XPD720 can support automatic wake-up of Type-C device insertion, intelligently identify the forward and reverse plug, and realize connection. The PD protocol integrated with XPD720 supports Biphase Mark Code (BMC), integrates hardware physical layer and protocol layer, and does not need software to participate in coding and decoding.

The XPD720 can support 36W output power at most. The PDO voltage of broadcast can be configured as 5V / 9V / 12V, and the APDO voltage range of 5V prog and 9V prog can be flexibly configured.

The XPD720 can be connected to AC-DC or DC-DC feedback pin through a sink / source current source to realize dynamic voltage regulation function. No matter the startup or voltage regulation process, it has soft start / voltage regulation function to realize smooth voltage transition.

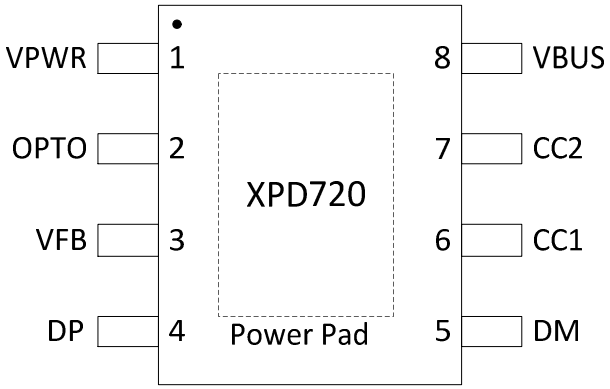
The XPD720 has a variety of built-in protection mechanisms to ensure equipment safety: including dynamic overvoltage, under voltage, over-current protection, which can adjust the protection point according to the working voltage or current requested by the equipment; start monitoring, which will monitor whether the VBUS port voltage is in a safe state; DP / DM and CC1 / CC2 overvoltage.

The XPD720 integrates a 10 m Ω VBUS path power switch and a dual discharge path, and integrates a constant voltage control loop. In case of an error, the XPD720 can shut down the output faster and return to a safe state.

The XPD720 can easily pass USB PD certification test without adding components.

The XPD720 is available in ESOP8 package, which can work without additional components, and provides optimal BOM cost characteristics.

5 Pin Description



NO.	NAME	Description
1	VPWR	External voltage source
2	OPTO	Opto drive
3	VFB	Current source/sink output for output voltage adjustment
4	DP	USB positive data line
5	DM	USB negative data line
6	CC1	Configuration channel interface pin to USB Type-C
7	CC2	Configuration channel interface pin to USB Type-C
8	VBUS	The voltage monitor for VBUS line, which is the high-side power conductor
Power Pad	GND	Power Ground

6 Ordering Information

Part Number	PDO and APDO configuring	Marking	Package
XPD720A	PDO:5V/3A, 9V/2.22A	XPD720 XXXXX+XX	ESOP8 4K/Disk
XPD720B	PDO:5V/3A, 9V/2.22A, 12V/1.67A		
XPD720B18	PDO: 5V/3A, 9V/2A, 12V/1.5A		
XPD720B20	PDO:5V/3A, 9V/2.25A, 12V/1.5A		
XPD720BP	PDO:5V/3A, 9V/2.22A, 12V/1.67A APDO1 : 3.3-5.9V/3A APDO2 : 3.3-11V/1.8A		
XPD720APS25	PDO:5V/3A, 9V/2.77A APDO1 : 3.3-5.9V/3A APDO2 : 3.3-11V/2.25A		
XPD720APS30	PDO:5V/3A, 9V/2.77A APDO1 : 3.3-5.9V/3A APDO2 : 3.3-11V/2.75A		
XPD720BP25	PDO:5V/3A, 9V/2.77A, 12V/2.08A APDO1 : 3.3-5.9V/3A APDO2 : 3.3-11V/2.25A		
Customizable	Customizable		

Marking Description

The first line，XPD720：Device Code；

The second line，XXXXX：Lot Number，XX：reserved。

* SCP protocol needs to be customized because the current exceeds 3A。

Selection Reference

	QC3.0	FCP/SCP	AFC	PD3.0	PPS	CV	A+C	SR	SR MOS	XPD-LINK
XPD618	√	√	√	√						
XPD636	√	√	√	√			√			
XPD720	√	√	√	√	√	√				
XPD738	√	√	√	√	√	√	√			
XPD737	√	√	√	√	√					√
XPD767	√	√	√	√	√		√			√
XPD818	√	√	√	√		√		√	√	
XPD819	√	√	√	√		√		√	√	
XPD865	√	√	√	√		√		√		

7 Specifications

7.1 Absolute Maximum Ratings (1)

PARAMETER		MAX	MIN	UNIT
Withstand Voltage（To PGND）	VPWR, VBUS, OPTO, CC1, CC2, DP, DM	-0.3	25	V
	Others	-0.3	7	V
Operating Junction Temperature	T_J	-40	150	℃
Storage Temperature Range	T_{STG}	-65	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Rating

SYMNOL	PARAMETER	VALUE	UNIT
V_{ESD}	HBM	±4000	V

ESD test is based on Human Body Model（HBM）。

7.3 Recommended Operating Condictions

PARAMETER		MIN	TYP	MAX	UNIT
VPWR	Input Supply Voltage	3.6		12	V
C_{VBUS}	VBUS Capacitance		1		μF
C_{VPWR}	VPWR Capacitance	4.7	10		μF
R_{FB1}	Feedback Pull-up Resistor		100		kΩ
R_{FB2}	Feedback Pull-down Resistor		33		kΩ
T_A	Operation Temperature Range	-40		85	℃

7.4 Thermal Resistance

SYMNOL	PARAMETER	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42	℃/W

7.5 Electrical Characteristics

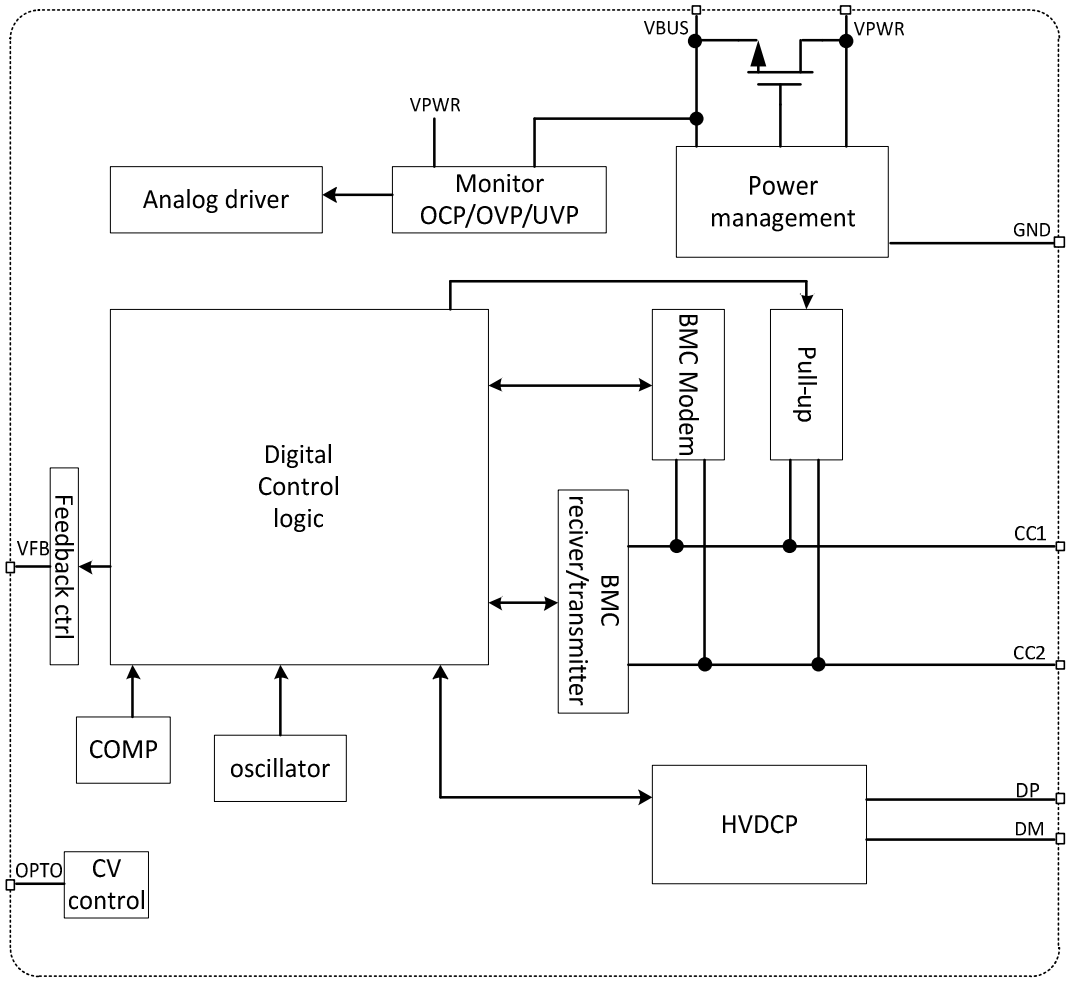
Unless otherwise stated in a specific test condition the following Conditions apply:T_J =25℃, 5V≤V_{VPWR}≤12V

PARAMETER		TEST CONDICTIONS	MIN	TYP	MAX	UNIT
Power Supply (VBUS, VPWR)						
V_{VPWR_TH}	VPWR UVLO threshold	Rising edge		3.3		V
		Falling edge		2.9		
		Hysteresis		0.4		
I_{SUPP}	Operating current while sink attached	VPWR=5V， VBUS=5V		2		mA
Voltage Protection (VBUS)						
V_{FOVP}	Fast OVP threshold always enabled	Ref to target voltage		+20%		V
V_{SOVP}	Slow OVP threshold	Ref to target voltage		+15%		V
Switch MOSFET						
R_{DSON}				10		mΩ
Transmitter (CC1, CC2)						
R_{TX}	Output resistance	During transmission		50		Ω
V_{TXHI}	Transmit HIGH			1.15		V
V_{TXLO}	Transmit LOW		-75		75	mV
t_{UI}	Bit unit interval			3.3		us
t_{BMC}	Rise/fall time of BMC	R_{load}=5.1k,C_{load}=1nF	300		600	ns
Receiver (CC1, CC2)						
V_{RXHI}	Receive HIGH		800	840	885	mV
V_{RXLO}	Receive LOW		485	525	570	
I_{RP_SRC}	CC1/CC2Broadcasting current	3A DFP mode, 0 $\leq V_{CCX} \leq$ 2.5V	304	330	356	uA
		1.5A DFP mode, 0 $\leq V_{CCX} \leq$ 1.5V	166	180	194	uA
OCP						
V_{ITRIP}		Ref to Power Capability(pd)		+30%		A
OTP (internal)						
T_{J1}	Die temperature	Temperature rising edge	135	145	155	℃
		Hysteresis		20		℃
HVDCP interface (DP, DM)						
$V_{DAT(REF)}$	Date Detect Voltage		0.25	0.325	0.4	V
$T_{GLITCH(DP)HIGH}$	DP High Glitch Filter Time		1	1.25	1.5	s
$T_{GLITCH(DM)LOW}$	DM Low Glitch Filter Time			1		ms
$T_{GLITCH(V)CHANGE}$	Output Voltage Glitch Filter Time		20	40	60	ms
$T_{GLITCH(CONT)CHANGE}$	Continuous Mode Glitch Filter Time		100	150	200	us

$R_{DAT(LKG)}$	DP Leakage Resistance		300	500	800	KΩ
$R_{DM(DWN)}$	DM Pull-Down Resistance		14.25	19.53	24.5	KΩ
$R_{ON(N1)}$	Switch SW1 on-resistance				100	Ω
$V_{TH(PD)}$	Output Device Connection Detection threshold		0.25	0.325	0.4	V
TD_{PD}	Output Device connection Detection Glitch Filter Time		120	160	200	ms
$\Delta I_{T(UP)}$	Up Current Step	R_{IREF}=100KΩ		2		uA
$\Delta I_{T(DO)}$	Down Current Step	R_{IREF}=100KΩ		2		uA
Apple 2.4A Mode						
$V_{DAT(2.7V)}$	D+/D- line output voltage		2.57	2.7	2.84	V
$R_{DAT(2.7V)}$	D+/D- line output Impedance			12		KΩ
FCP Mode						
V_{TX-VOH}	D- FCP TX Valid High			2.7		V
V_{TX-VOL}	D- FCP TX Valid Low				0.3	V
V_{RX-VIH}	D- FCP RX Valid High			1.2		V
V_{RX-VIL}	D- FCP RX Valid High			0.9		V
Trise	FCP Pulse Rise Time	10% - 90%			2.5	us
Tfall	FCP Pulse Fall Time	90% - 10%			2.5	us

8 Application Information

8.1 Function Module diagram

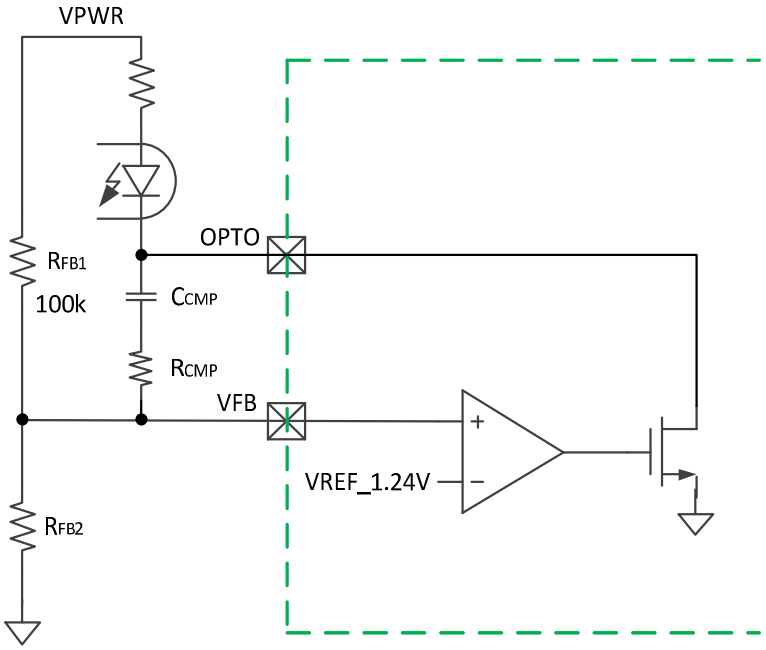


8.2 VPWR and VBUS

VPWR is the input power of VBUS with USB Type-C and also the power supply of chip. The VPWR is connected to the power output of the former AC-DC or DC-DC. It is recommended that the ground capacitance C_{VPWR} close to VPWR, and the typical value of C_{VPWR} is 10 μ F. It is recommended to connect 1 μ f ground capacitance C_{VBUS} close to VBUS.

8.3 Constant Voltage Loop and OPTO、VFB

The XPD720 is internally integrated with a constant voltage operational amplifier and forms a constant voltage loop (CV) through opto and VFB, as shown in the figure below. The traditional TL431 can be omitted by directly driving the optocoupler by the opto port. Opto can withstand voltage above 20V.



Constant voltage loop (CV) needs to be compensated externally. Compensation resistance R_{CMP} and compensation capacitor C_{CMP} are determined by specific application. The internal reference voltage of VFB is 1.24 V. The voltage divider R_{FB1} of the feedback resistance network on the VPWR must be connected to 100kΩ, with an accuracy of 1%.

If the initial output voltage is set to 5V, the other voltage divider R_{FB2} is 33K, with an accuracy of 1%. It can be calculated by the following formula:

$$R_{FB2} = \frac{1.24 * R_{FB1}}{V_{PWR} - 1.24}$$

The initial output voltage can be changed by adjusting the value of R_{FB2}.

8.4 Current Sense

The XPD720 built-in current detection circuit, real-time detection of Type-C port current. The default over-current protection point of Type-C port is 130% of PDO broadcast current

8.5 Line Loss Compensation

The XPD720 has the function of line loss compensation, which can increase the output voltage in proportion (i.e. compensation coefficient) according to the output current. The compensation coefficient can be configured internally. The compensation coefficient of the XPD720 is set at 60mV / A. If the output voltage of front-end power supply is 5V under

no-load, the output voltage of front-end power supply will increase to 5.18V when the output current is 3A.

8.6 Reliability

Because CC1 / CC2 / DP / DM pin is directly connected to USB port, it is easy to be short circuited with power supply in the process of use, causing damage to the chip. In order to enhance the safety and reliability of the XPD720, the withstand voltage value of CC1 / CC2 / DP / DM pin is increased to more than 20V.

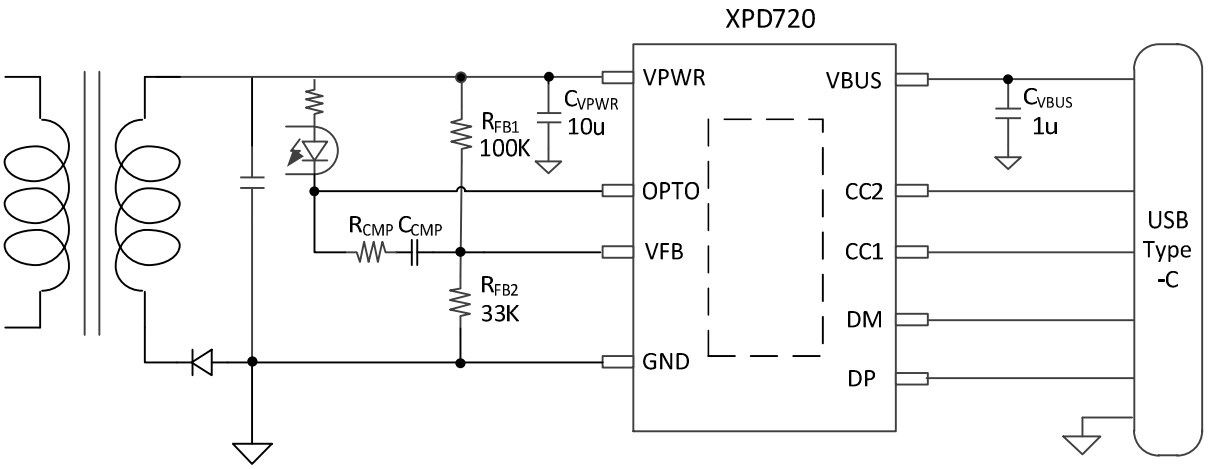
The XPD720 has complete OVP / OCP / UVP protection function. The OVP / OCP / UVP protection threshold will be adjusted according to the voltage selected by the equipment to maximize the safety of the equipment

The XPD720 has built-in VPWR and VBUS energy discharge channels, which can open and discharge the power supply energy of VPWR and VBUS under certain conditions.

When the junction temperature of the XPD720 reaches 145 ℃, the output will be turned off, and when it drops to 125 ℃, the protection will be released and the work will start again.

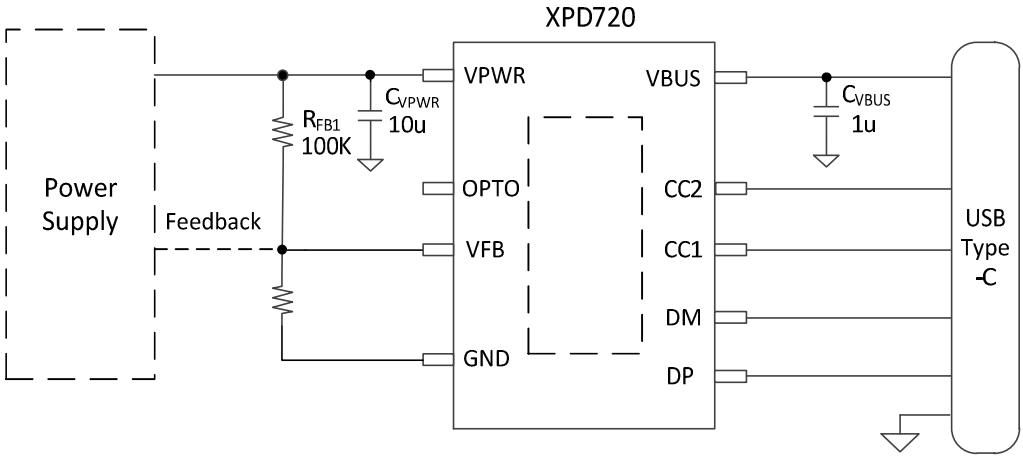
9 Application Circuit

9.1 AC-DC Application Circuit



The component parameters shown in the figure are for reference and can be adjusted according to the actual application. Refer to section 8.3 to set the values of feedback network divider resistance R_{FB1} and R_{FB2}, and the values of compensation network R_{CMP} and C_{CMP}.

9.2 DC-DC Application Circuit

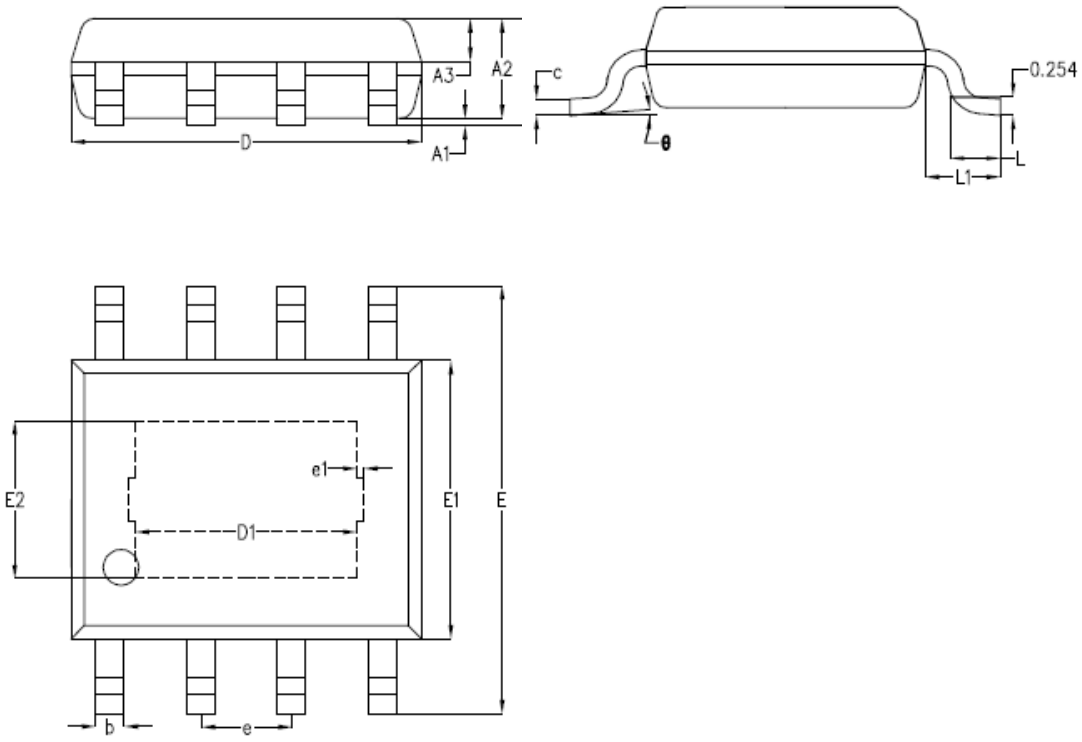


The component parameters shown in the figure are for reference and can be adjusted according to the actual application. The voltage divider R_{FB1} of feedback resistance network on VPWR must be connected with 100kΩ

9.3 PCB layout Guidelines

1. Input capacitor C_{VPWR} and output capacitor C_{VBUS} should be close to the chip ;
2. Heating element as far as possible away from XPD720
3. Try to avoid the interference of VFB connection. R_{CMP} and C_{CMP} of compensation network are placed close to VFB pin.

10 Packge Information



SYMBOL	MIN	TYP	MAX
A	-	1.50	1.55
A1	-	0.10	0.15
A2	1.35	1.40	1.45
A3	0.55	0.60	0.65
b	0.35	0.40	0.45
c	0.17	0.22	0.25
D	4.85	4.90	4.95
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.60	0.65	0.70
L1	1.05BSC		
θ	0°	4°	6°

