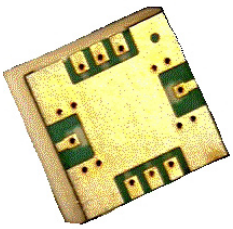
AMMP-6232
18 to 32 GHz GaAs High Linearity LNA in SMT Package

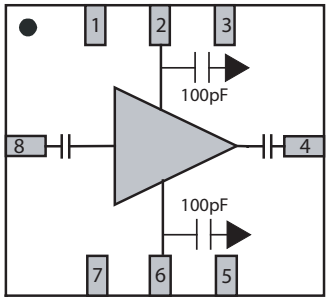
Data Sheet



Description

Avago's AMMP-6232 is an easy-to-use broadband, high gain, high linearity Low Noise Amplifier in a surface mount package. The wide band and unconditionally stable performance makes this MMIC ideal as a primary or sub-sequential low noise block or a transmitter driver. The MMIC has 4 gain stages and requires a 4V, 138mA power supply for optimal performance. Since this MMIC covers several bands, it can reduce part inventory and increase volume purchase options The MMIC is fabricated using PHEMT technology. The surface mount package eliminates the need of "chip & wire" assembly for lower cost. This MMIC is fully SMT compatible with backside grounding and I/Os.

Pin Connections (Top View)



Top view
Package base: GND

Pin	Function
1	
2	Vdd
3	
4	RFout
5	
6	Vg
7	
8	RFin

Features

- Surface Mount Package, 5.0 x 5.0 x 1.25 mm
- Single Power Supply Pin
- Unconditionally Stable
- 50Ohm Input and Output Match

Specifications (Vdd = 4.0V, Idd = 138mA)

- RF Frequencies: 18 - 32 GHz
- High Output IP3: 29dBm
- High Small-Signal Gain: 23dB
- Typical Noise Figure: 3dB

Applications

- Microwave Radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops
- Commercial grade military

Note:
1. This MMIC uses depletion mode pHEMT devices.
2. Negative voltage is used for the gate bias

Attention:
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control

Absolute Maximum Ratings [1]

Parameters / Conditions	Symbol	Unit	Max
Drain to Ground Voltage	Vdd	V	5.5
Gate-Drain Voltage	Vgd	V	-8
Drain Current	Idd	mA	200
Gate Bias Voltage	Vg	V	+0.8
Gate Bias Current	Ig	mA	1
RF CW Input Power Max	Pin	dBm	10
Max channel temperature	Tch	C	+150
Storage temperature	Tstg	C	-65 +150
Maximum Assembly Temp	Tmax	C	260 for 20s

1. Operation in excess of any of these conditions may result in permanent damage to this device. The absolute maximum ratings for Vdd, Vgd, Idd, Vg, Ig and Pin were determined at an ambient temperature of 25°C unless noted otherwise.

DC Specifications/ Physical Properties [2]

Parameter and Test Condition	Symbol	Unit	Min	Typ	Max
Drain Supply Current (Vd=4.0 V)	Idd	mA		135	150
Drain Supply Voltage	Vd	V	3	4	5
Gate Bias Current	Ig	mA		0.1	
Gate Bias Voltage	Vg	V	-1.1	-0.95	-0.8
Thermal Resistance(3)	θjc	°C/W		35.1	

2. Ambient operational temperature TA=25°C unless noted
3. Channel-to-backside Thermal Resistance (Tchannel = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temp. (Tb) = 25°C calculated from measured data.

AMMP-6232 RF Specifications [4]

TA= 25°C, Vdd = 4.0 V, Idd =135 mA, Zo=50 Ω

Parameters and Test Conditions	Freq. (GHz)	Symbol	Units	Minimum	Typical	Maximum	Sigma
Small-Signal Gain[5]	20, 26, 29	Gain	dB	19	23		
Noise Figure into 50Ω[5]	20, 26, 29	NF	dB		3	4.5	
Output Power at 1dB Gain Compression		P-1dB	dBm		18		
Output Power at 3dB Gain Compression		Psat	dBm		20		
Output Third Order Intercept Point		OIP3	dBm		29		
Isolation		Iso	dB		-45		
Input Return Loss		RLin	dB		-10		
Output Return Loss		RLout	dB		-10		

4. Refer to characteristic plots for detailed individual frequency performance.
5. All tested parameters guaranteed with measurement accuracy ± 1.5dB for gain and ±0.4dB for NF.

AMMP-6232 Typical Performance [1], [2]

(T_A = 25°C, Vdd=4V, Idd=138mA, Z_{in} = Z_{out} = 50 Ω unless noted)

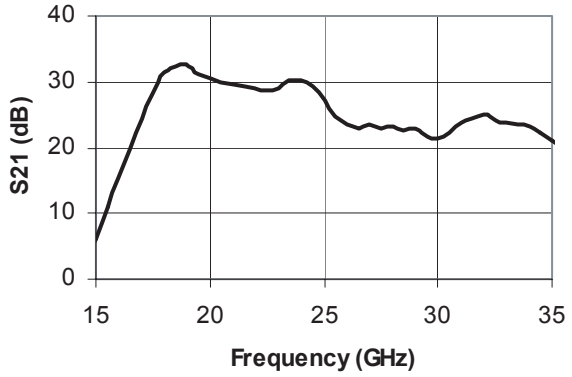


Figure 1. Small-signal Gain

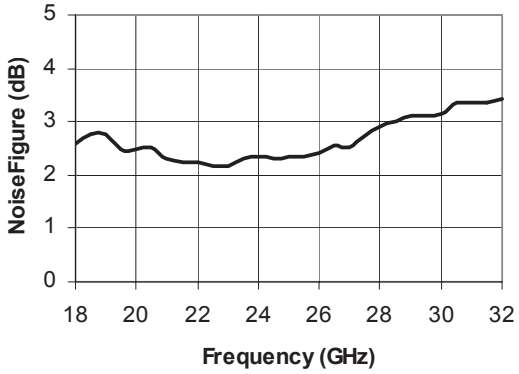


Figure 2. Noise Figure

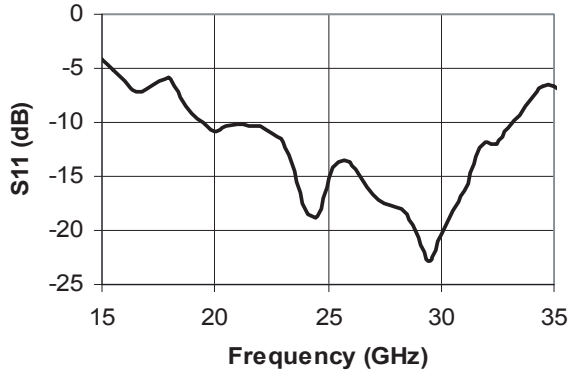


Figure 3. Input Return Loss

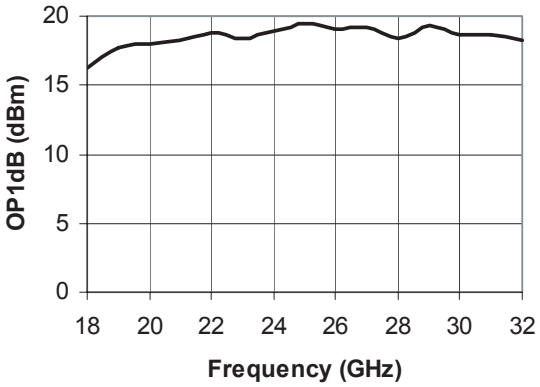


Figure 4. Output P-1dB

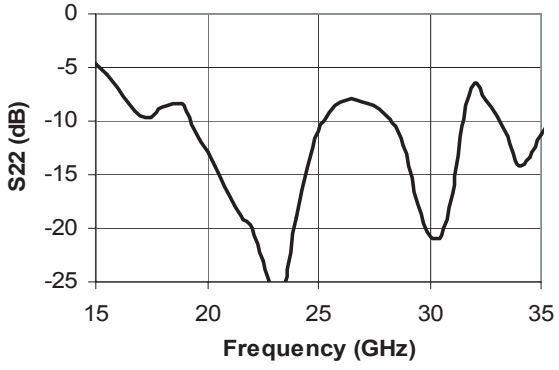


Figure 5. Output Return Loss

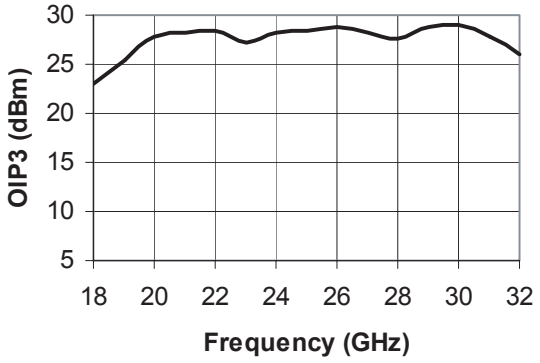


Figure 6. Output IP3

Note:
1. S-parameters are measured on R&D Eval Board as shown in Figure 20. Effects of connectors and board traces are included in results.
2. Noise Figure is measured on R&D Eval Board as shown in Figure 20, and with a 3dB pad at the input. Board and Connector losses are already de-embeded from the data.

AMMP-6232 Typical Performance (cont.)

(T_A = 25°C, Vdd=4V, Idd=138mA, Z_{in} = Z_{out} = 50 Ω unless noted)

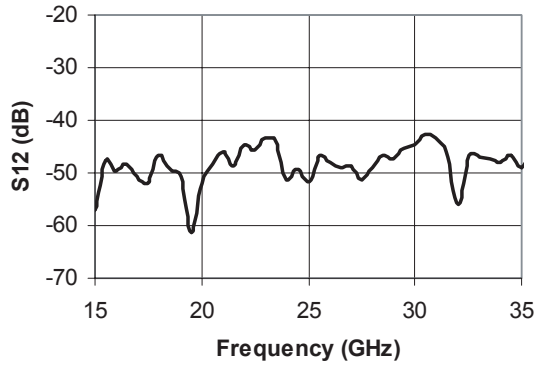


Figure 7. Isolation

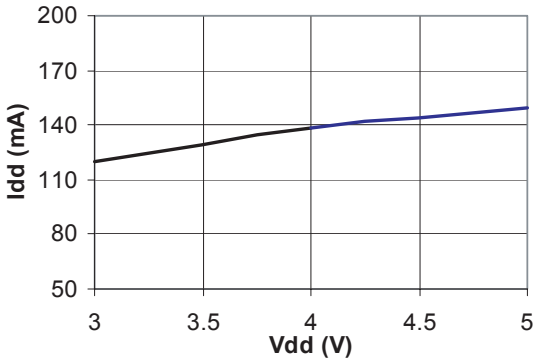


Figure 8. Total Current

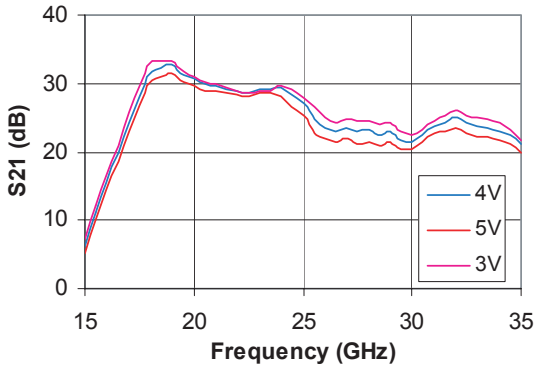


Figure 9. Gain over Vdd

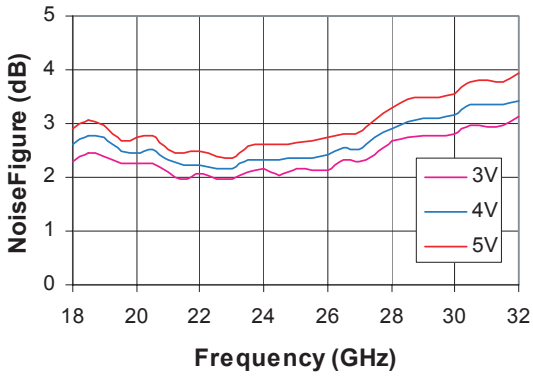


Figure 10. Noise Figure over Vdd

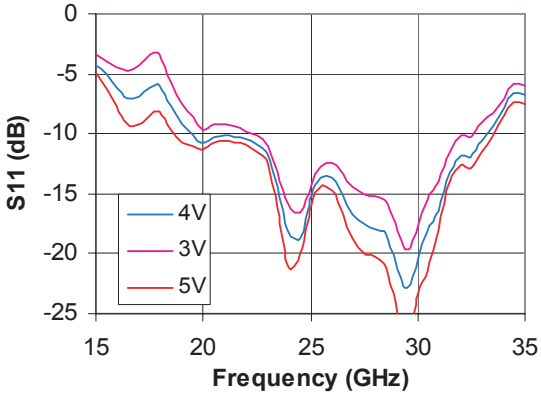


Figure 11. Input Return Loss Over Vdd

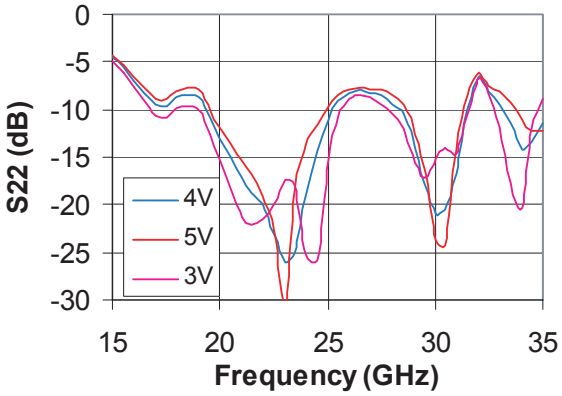


Figure 12. Output Return Loss Over Vdd

AMMP-6232 Typical Performance (cont.)

(T_A = 25°C, Vdd=4V, Idd=138mA, Z_{in} = Z_{out} = 50 Ω unless noted)

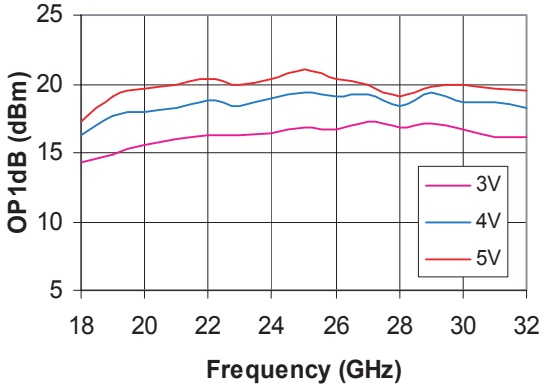


Figure 13. Output P-1dB over Vdd

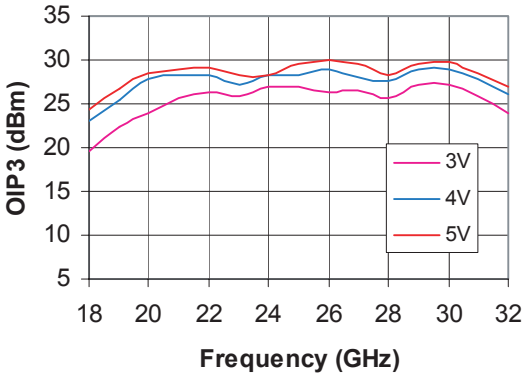


Figure 14. Output IP3 Over Vdd

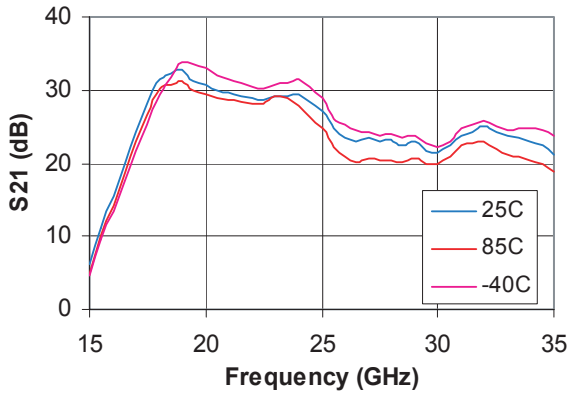


Figure 15. Gain over Temp

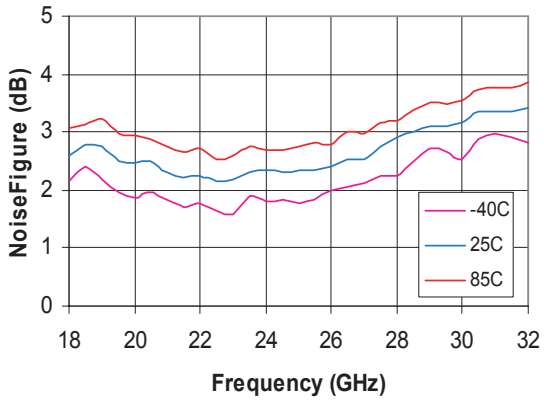


Figure 16. Noise Figure over Temp

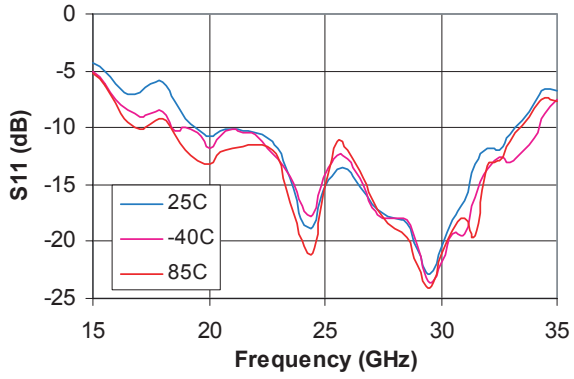


Figure 17. Input Return Loss Over Temp

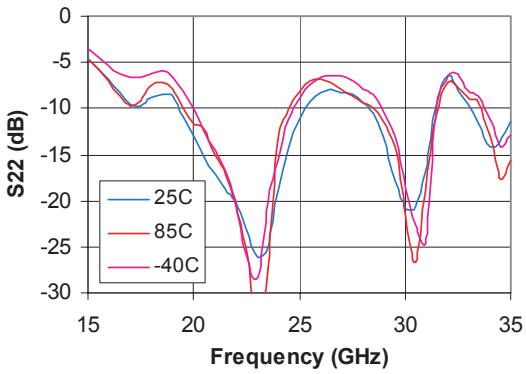


Figure 18. Output Return Loss Over Temp

AMMP-6232 Application and Usage

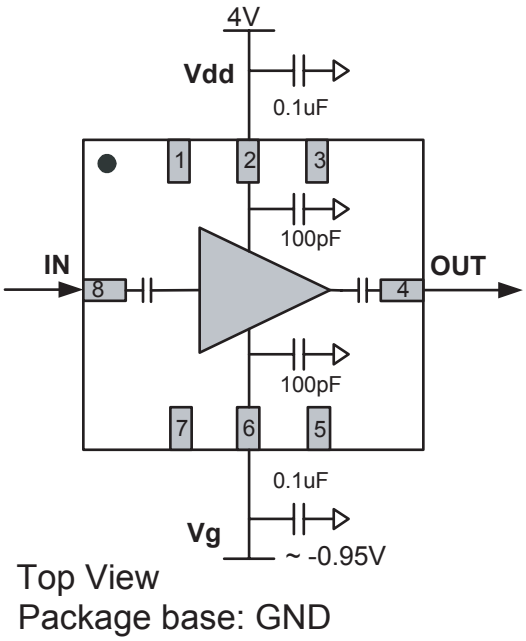


Figure 19. Usage of the AMMP-6232

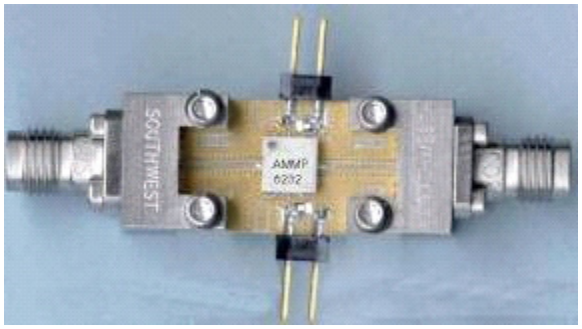


Figure 20. Evaluation/Test Board (available to qualified customer request)

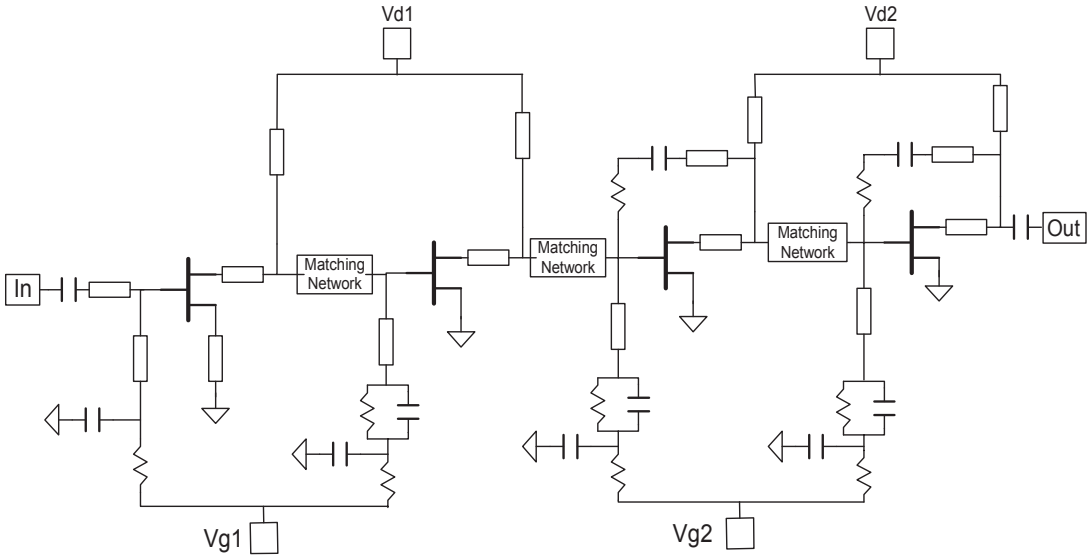


Figure 21. Simplified AMMP-6232 Schematic

Biasing and Operation

The AMMP-6232 is normally biased with a positive drain supply connected to the VDD pin and a negative gate bias through bypass capacitors as shown in Figure 19. The recommended drain supply voltage is 4 V and the gate bias is approximately -0.95V to get the corresponding drain current of 138mA. It is important to have 0.1uF bypass capacitors and the capacitor should be placed as close to the component as possible. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise (Topt) matching.

After adjusting the gate bias to obtain 138mA at Vdd = 4V, the AMMP-6232 can be safely biased at 3V or 5V (while fixing the gate bias) as desired. At 4V, the performance is an optimal compromise between power consumption, gain and power/linearity. It is both applicable to be used as a low noise block or driver. At 3V, the amplifier is ideal as a front end low noise block where linearity is not highly required. At 5V, the amplifier can provide 1 to 2dBm more output power for LO or transmitter driver applications where high output power and linearity are often required.

Refer the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Recommended SMT Attachment for 5x5 Package

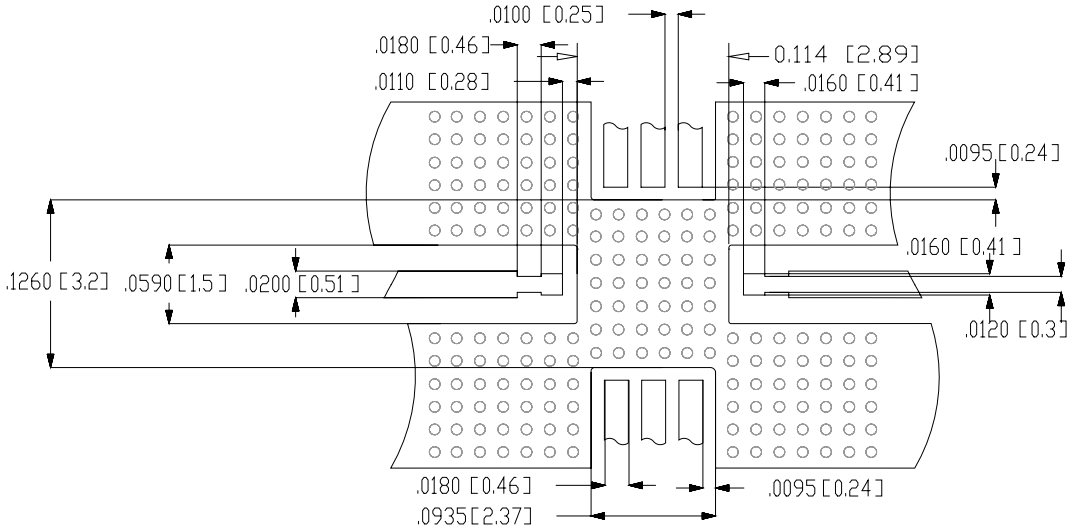


Figure 22a. Suggested PCB Land Pattern and Stencil Layout

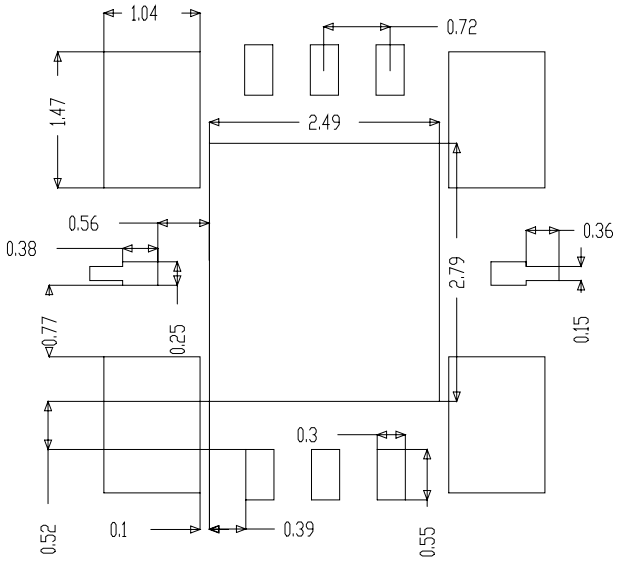


Figure 22b. Stencil Outline Drawing (mm)

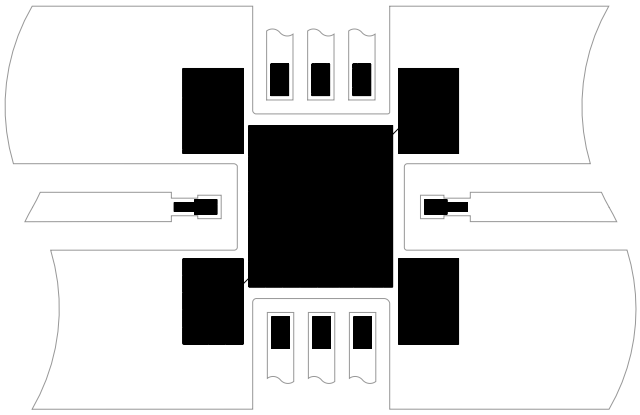


Figure 22c. Combined PCB and Stencil Layouts

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

Manual Assembly

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers.
- Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Neither Conductive epoxy or hand soldering is recommended.
- Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp. to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.

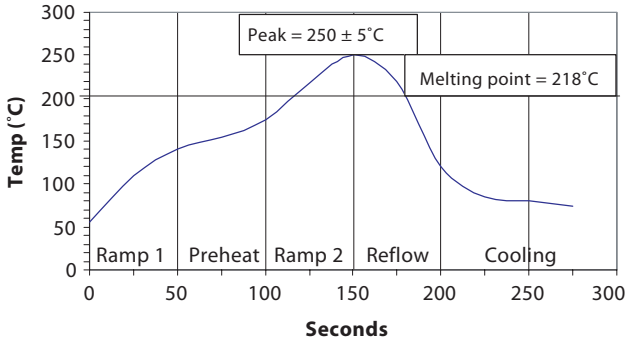


Figure 23. Suggested Lead-Free Reflow Profile for SnAgCu Solder Paste

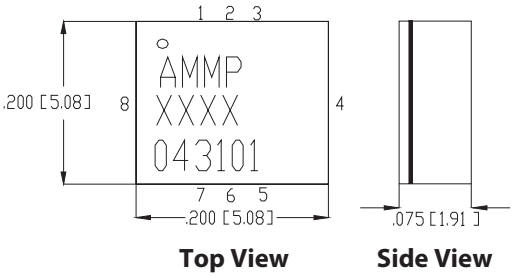
A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 22. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 23. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 1 will vary among different solder pastes from different manufacturers and is shown here for reference only.

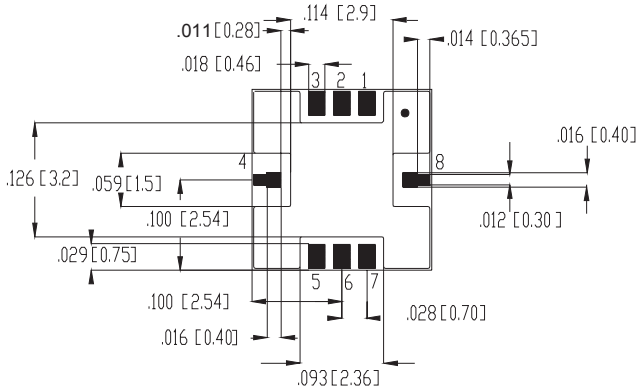
AMMP-6232 Part Number Ordering Information

Part Number	Devices Per Container	Container
AMMP-6232-BLKG	10	Antistatic bag
AMMP-6232-TR1G	100	7" Reel
AMMP-6232-TR2G	500	7" Reel

Package, Tape & Reel, and Ordering Information



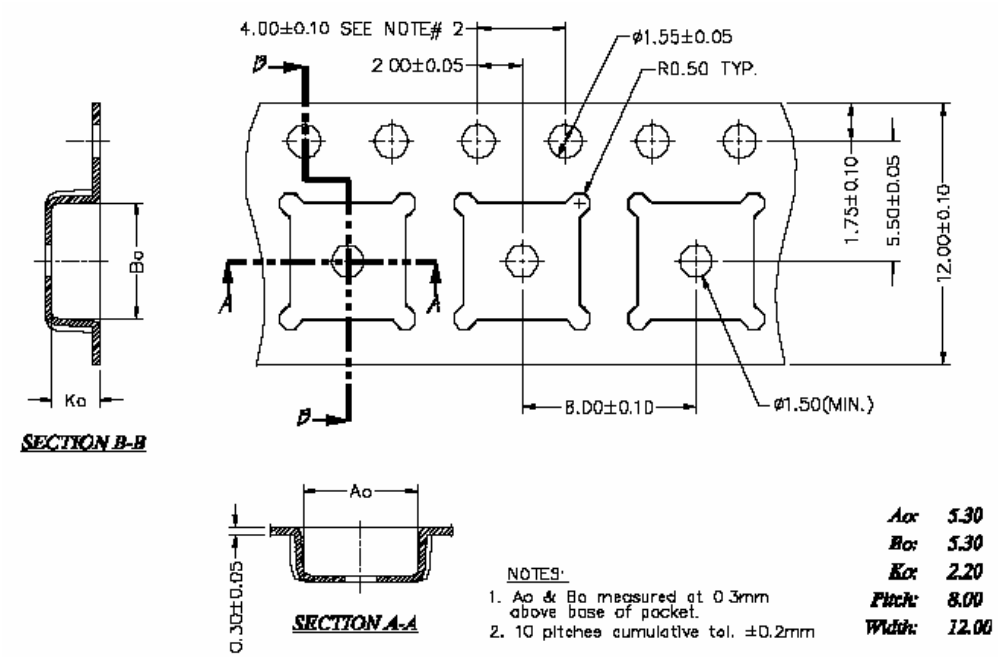
Top View **Side View**

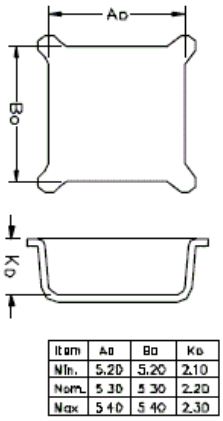


Back View

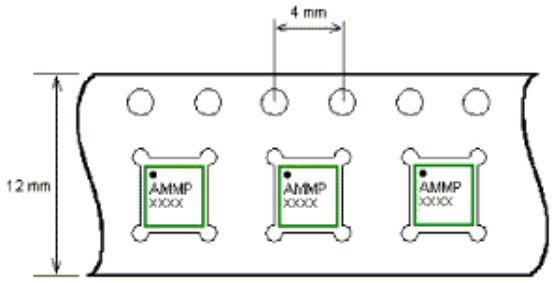
NOTES:
DIMENSIONS ARE IN INCHES [MILIMETERS]
ALL GROUNDS MUST BE SOLDERED TO PCB RF
Material is Rogers RO4350, 0.010" thick

Carrier Tape and Pocket Dimensions





Item	Ao	Bo	Ko
Min.	5.20	5.20	2.10
Nom.	5.30	5.30	2.20
Max	5.40	5.40	2.30



For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0491EN - June 12, 2007