P-Channel MOSFET MEM2301M3

General Description

MEM2301M3G Series P-channel enhancement mode field-effect transistor ,produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications, and low power dissipation, and low power dissipation in a very small outline surface mount package.

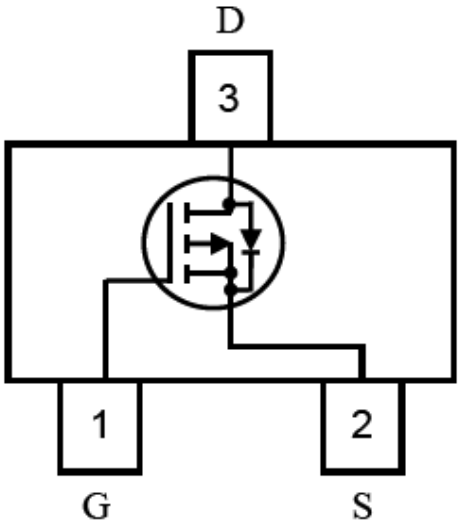
Features

- -20V/-2.8A

  $R_{DS(ON)}$ =93mΩ@ V_{GS}=-4.5V,I_D=-2.8A

  $R_{DS(ON)}$ =113mΩ@ V_{GS}=-2.5V,I_D=-2A
- High Density Cell Design For Ultra Low On-Resistance
- Subminiature surface mount package:SOT23-3L

Pin Configuration



Typical Application

- Power management
- Load switch
- Battery protection

Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	-2.8	A
	T_A=70℃		-1.8	
Pulsed Drain Current[1,2]		I_{DM}	-10	A
Total Power Dissipation	T_A=25℃	P_D	0.7	W
	T_A=70℃		0.45	
Operating Temperature Range		T_{Opr}	150	℃
Storage Temperature Range		T_{stg}	-65/150	℃

Thermal Characteristics

Parameter	Symbol	MAX.	Unit
Thermal Resistance,Junction-to-Ambient[3]	$R_{\theta JA}$	145	℃/W

Electrical Characteristics

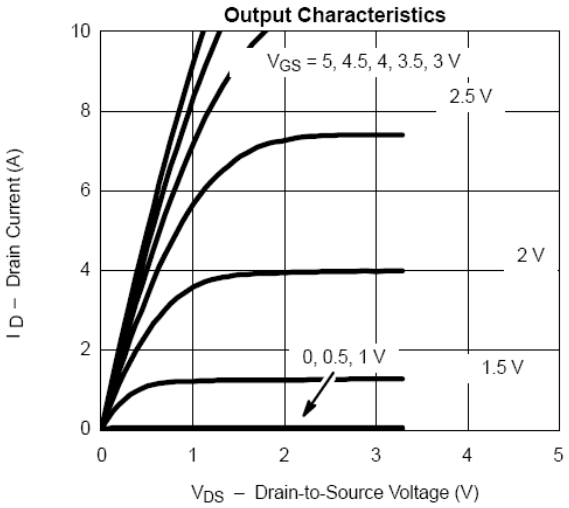
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250uA	-20	-23		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250uA	-0.4	0.58	-1	V
Gate-Body Leakage	I_{GSS}	V_{DS}=0V，V_{GS}=8V		0.2	100	nA
		V_{DS}=0V，V_{GS}=-8V		-0.2	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V V_{GS}=0V		-1.5	-100	nA
Static Drain-Source On-Resistance	$R_{DS(ON)1}$	V_{GS}=-4.5V,I_D=-2.8A		93	110	mΩ
	$R_{DS(ON)2}$	V_{GS}=-2.5V,I_D=-2A		113	140	mΩ
Forward Transconductance	g_{FS}	V_{DS} = –5 V, I_D = –2.8 A		6.5		S
Source-drain (diode forward) voltage	V_{SD}	V_{GS}=0V,I_S=-1A			-1.2	V
Dynamic Characteristics						
Input Capacitance	Ciss	V_{DS} = -6V,		500		pF
Output Capacitance	Coss	V_{GS} = 0 V,		115		
Reverse Transfer Capacitance	Crss	f = 1 MHz		60		
Switching Characteristics						
Turn-On Delay Time	td(on)	V_{DD} = -6 V,		5	25	ns
Rise Time	tr	I_D=-1 A,		30	60	
Turn-Off Delay Time	td(off)	V_{GEN} = -4.5 V,		25	60	
Fall-Time	tf	Rg = 6 Ω		10	60	
Total Gate Charge	Qg	V_{DS} = -6 V,		4.0	10	nc
Gate-Source Charge	Qgs	V_{GS} = -4.5 V,		0.8		
Gate-Drain Charge	Qgd	I_D = -2.8A		0.8		

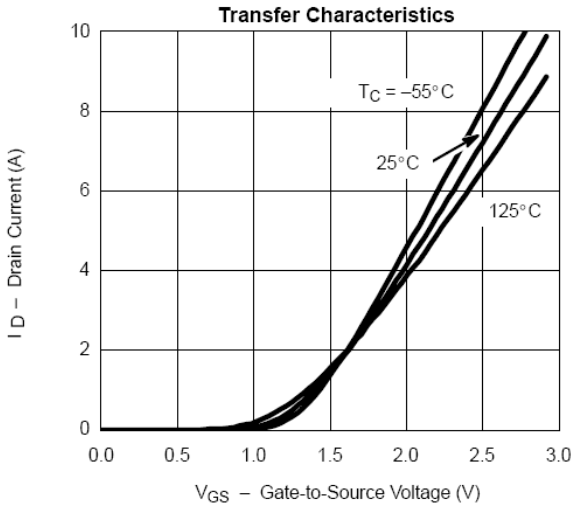
1、Pulse width limited by maximum junction temperature.

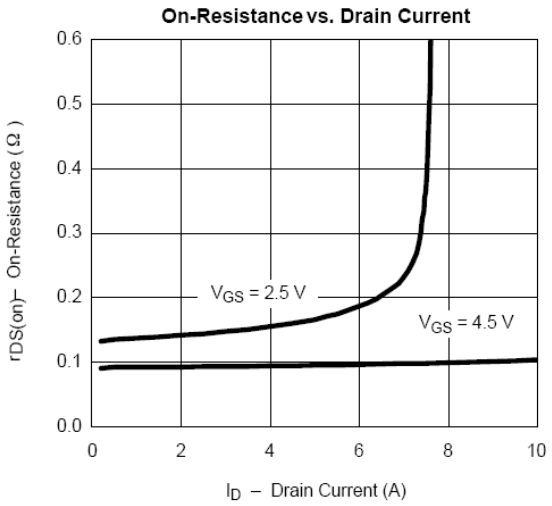
2、Pulse test: PW ≤300 us duty cycle ≤2%.

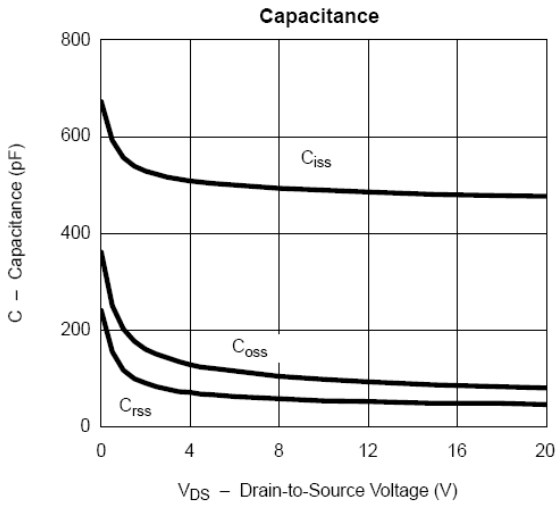
3、Surface Mounted on FR4 Board, t ≤ 5 sec.

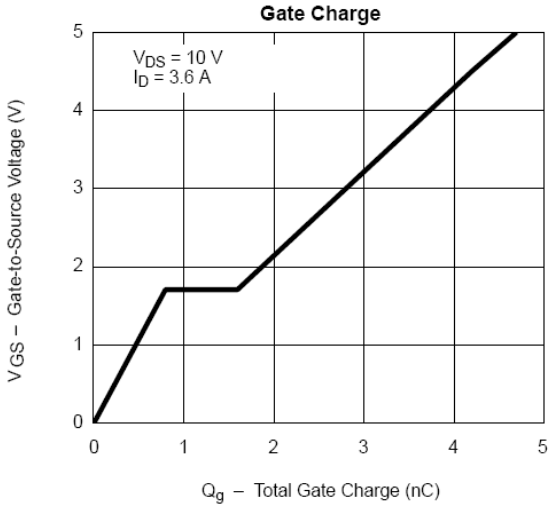
Typical Performance Characteristics

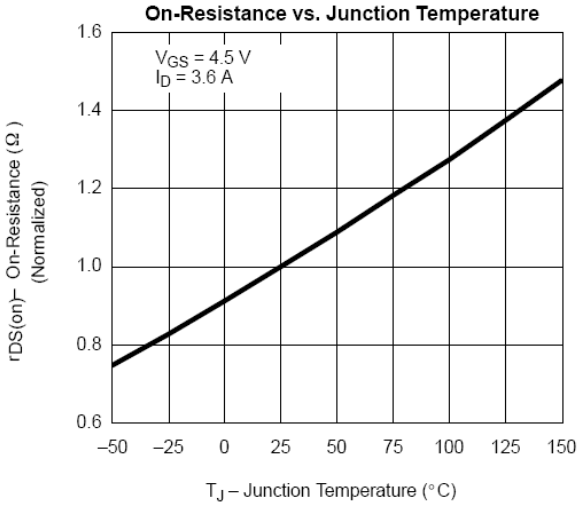




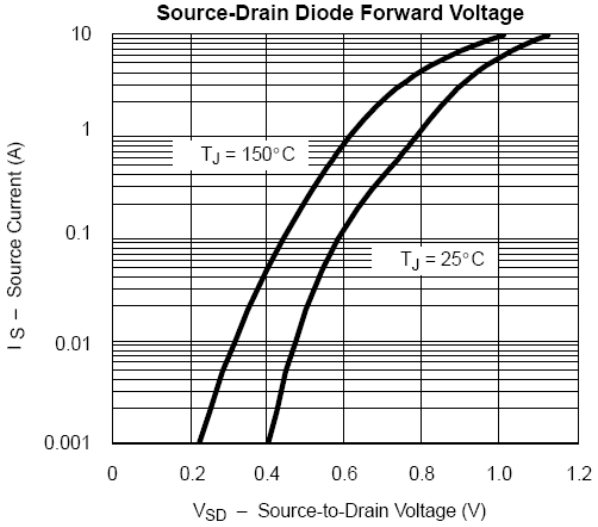




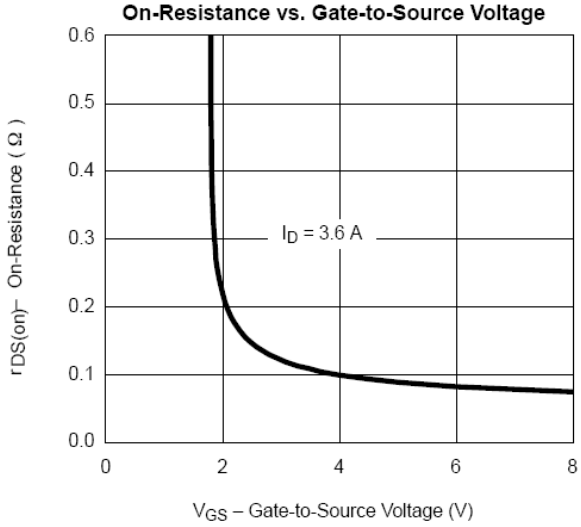




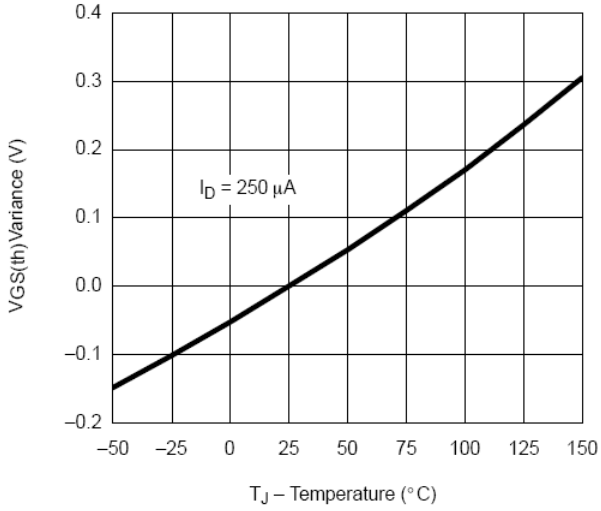
Source-Drain Diode Forward Voltage



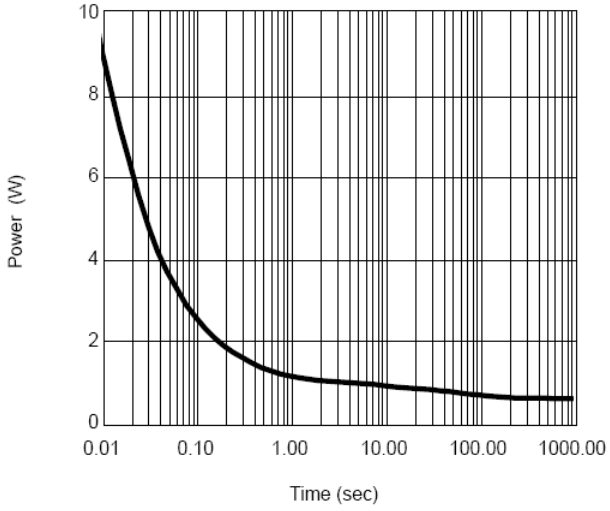
On-Resistance vs. Gate-to-Source Voltage



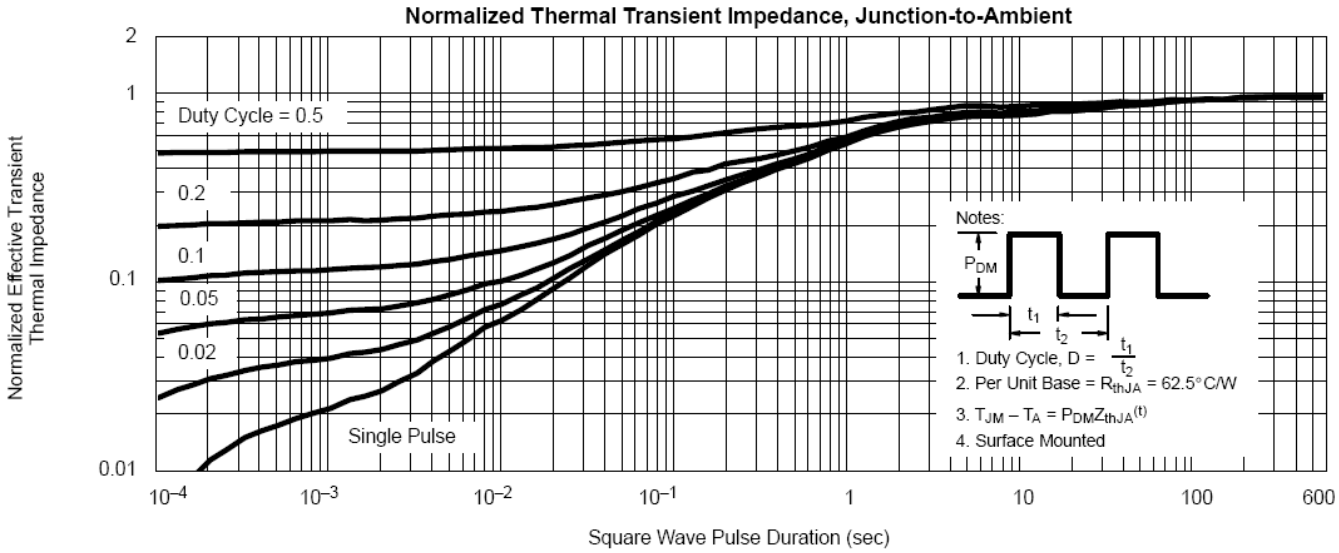
Threshold Voltage



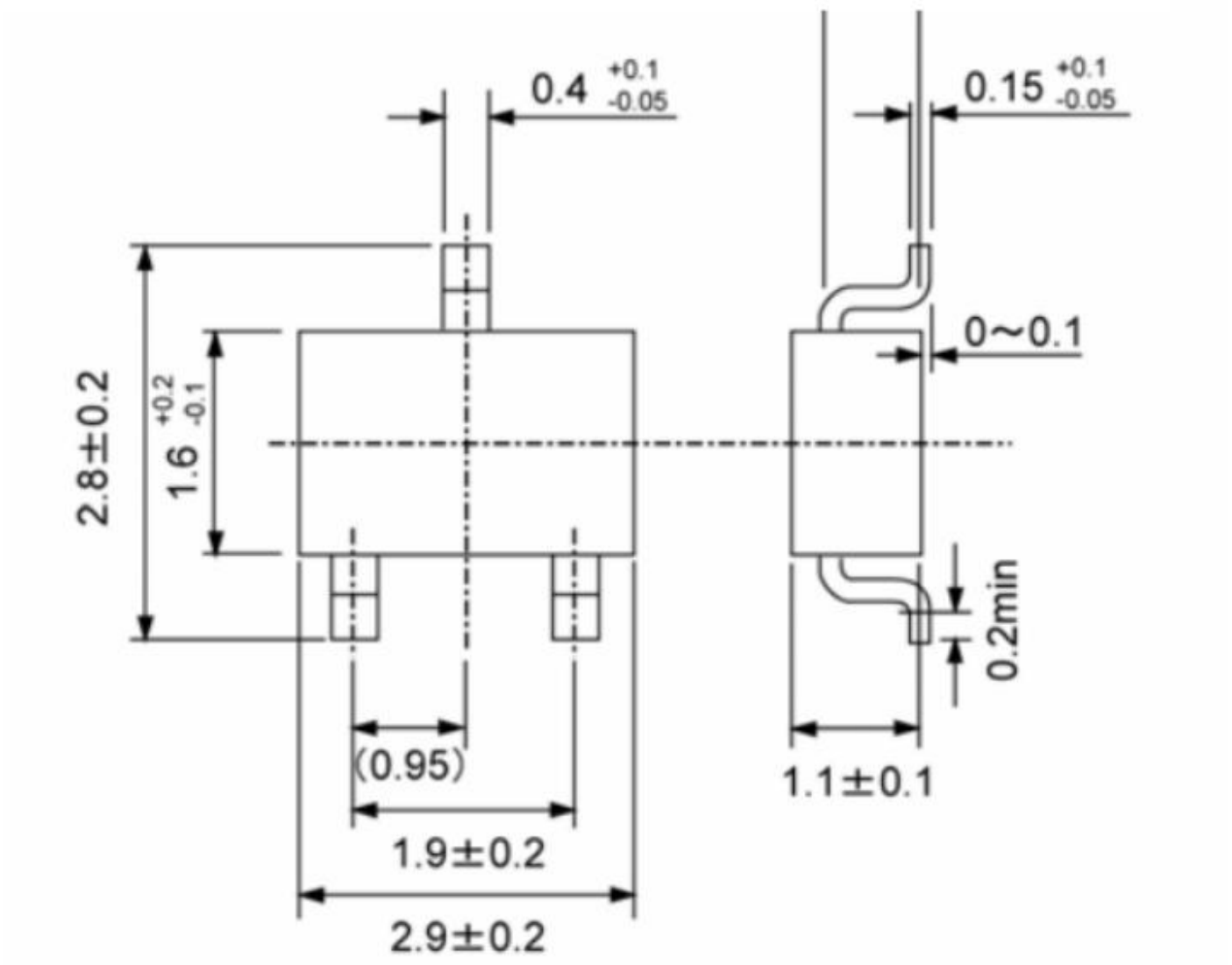
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Package Information



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