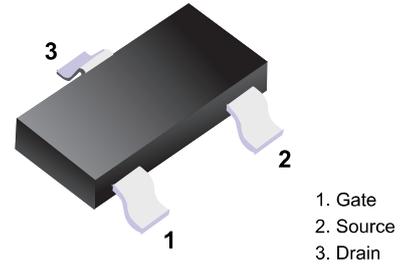


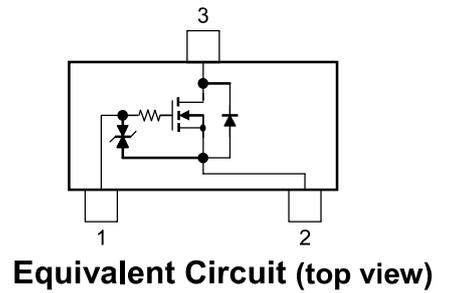
■ **N-Channel Enhancement Mode**

■ **Features**

- ESD protected gate
- Low ON-resistance
- $R_{DS(on)} = 2.8 \Omega$ (typ.) (@ $V_{GS} = 10 V$)
- $R_{DS(on)} = 3.1 \Omega$ (typ.) (@ $V_{GS} = 5 V$)
- $R_{DS(on)} = 3.2 \Omega$ (typ.) (@ $V_{GS} = 4.5 V$)



■ **Simplified outline(SOT23-3L)**



■ **MARKING**

Marking	A27K
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■ **Absolute Maximum Ratings (Ta = 25°C)**

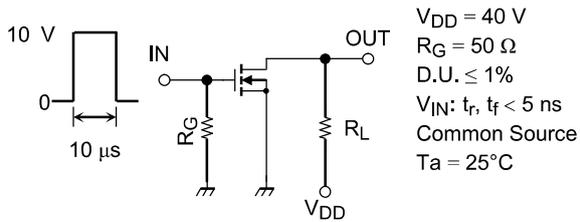
Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current (Note1)	DC	I_D	200
	Pulse	I_{DP} (Note 2)	760
Power dissipation	P_D (Note 3)	320	mW
	P_D (Note 4)	1000	
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to 150	°C

■ Electrical Characteristics (Ta = 25°C, Otherwise specified)

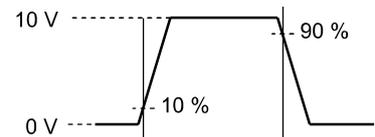
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 250 \mu A, V_{GS} = 0 V$	60	—	—	V
Drain cutoff current	I_{DSS}	$V_{DS} = 60 V, V_{GS} = 0 V$	—	—	1	μA
		$V_{DS} = 60 V, V_{GS} = 0 V, T_j = 150 ^\circ C$	—	—	200	
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16 V, V_{DS} = 0 V$	—	—	± 2	μA
		$V_{GS} = \pm 10 V, V_{DS} = 0 V$	—	—	± 0.5	
		$V_{GS} = \pm 5 V, V_{DS} = 0 V$	—	—	± 0.1	
Gate threshold voltage	V_{th}	$I_D = 250 \mu A, V_{DS} = V_{GS}$	1.1	—	2.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10 V, I_D = 200 mA$ (Note 5)	—	450	—	mS
Drain-source ON-resistance	$R_{DS(ON)}$ (Note 5)	$I_D = 100 mA, V_{GS} = 10 V$	—	2.8	3.9	Ω
		$I_D = 100 mA, V_{GS} = 10 V, T_j = 150 ^\circ C$	—	5.4	8.1	
		$I_D = 100 mA, V_{GS} = 5 V$	—	3.1	4.4	
		$I_D = 100 mA, V_{GS} = 4.5 V$	—	3.2	4.7	
Total Gate Charge	$Q_{G(tot)}$	$V_{DS} = 30 V, I_D = 200 mA$ $V_{GS} = 4.5 V$	—	0.27	0.35	nC
Gate-Source Charge	Q_{GS}		—	0.08	—	
Gate-Drain Charge	Q_{GD}		—	0.08	—	
Input capacitance	C_{iss}	$V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz$	—	11	17	pF
Output capacitance	C_{oss}		—	3	—	
Reverse transfer capacitance	C_{rss}		—	0.7	—	
Switching time	Turn-on delay time	$t_{d(on)}$	—	2	4	ns
	Rise time	t_r	—	3	—	
	Turn-off delay time	$t_{d(off)}$	—	7	14	
	Fall time	t_f	—	24	—	
Drain-source forward voltage	V_{DSF}	$I_D = -115 mA, V_{GS} = 0 V$ (Note 5)	—	-0.87	-1.2	V

Switching Time Test Circuit

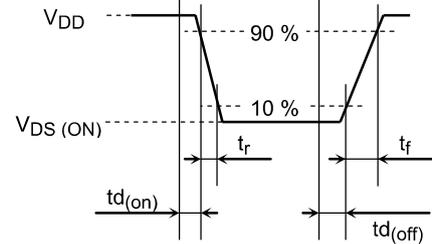
(a) Test Circuit



(b) V_{IN}



(c) V_{OUT}



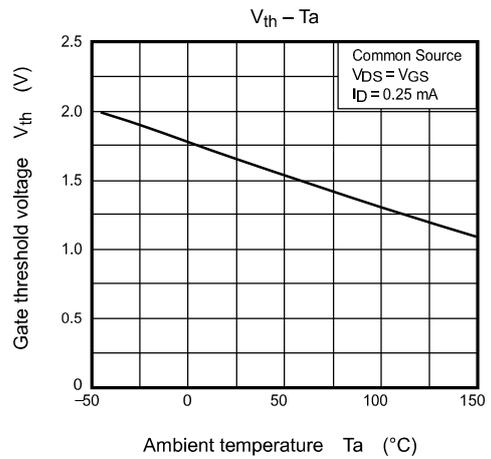
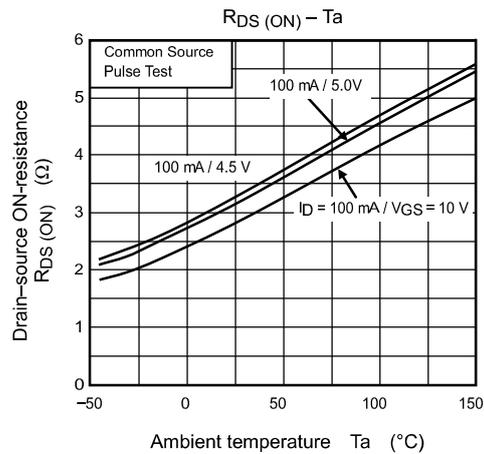
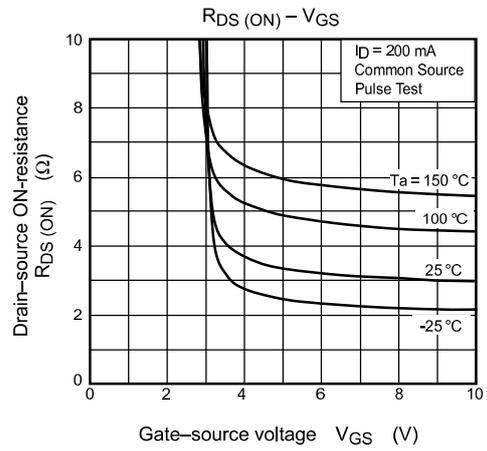
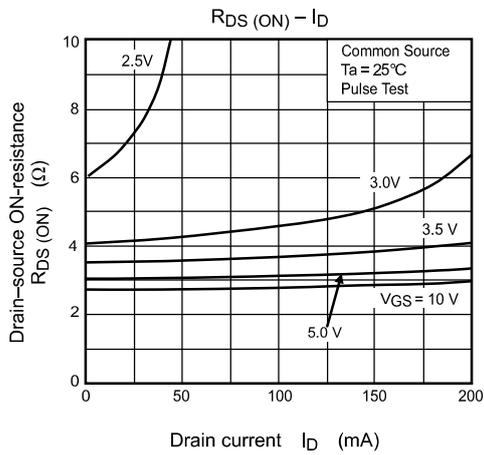
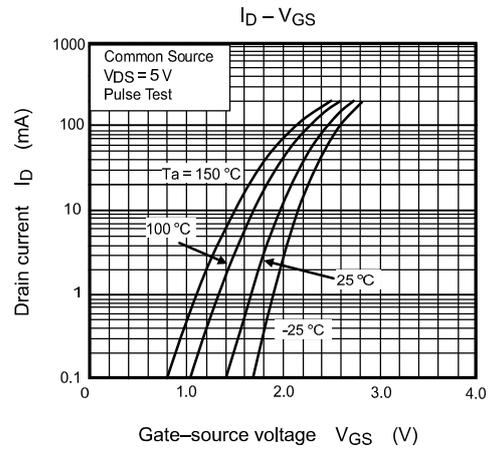
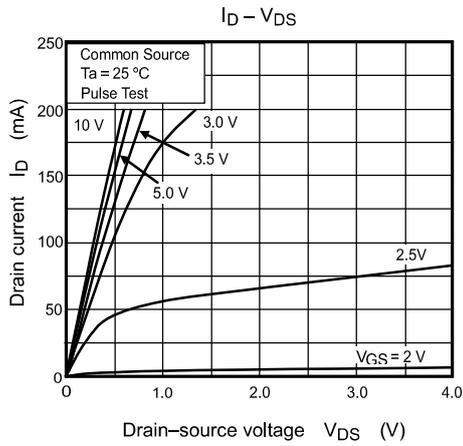
Notice of Usage

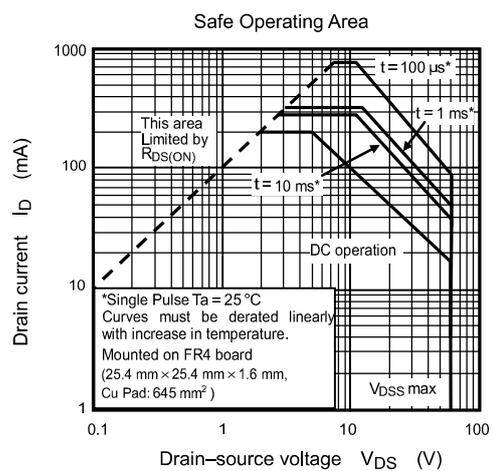
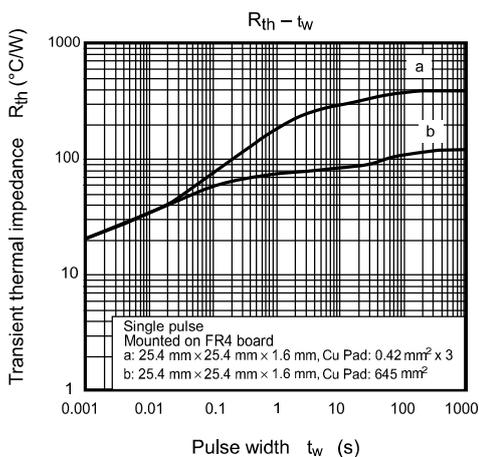
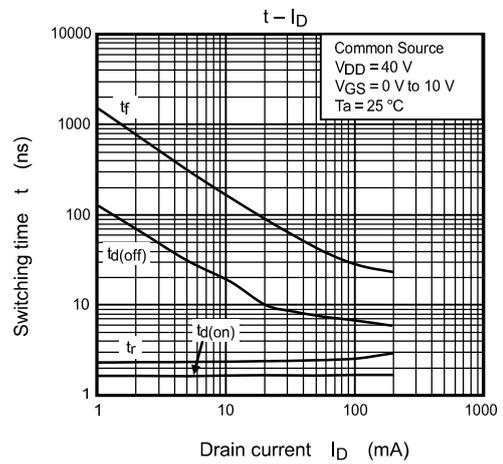
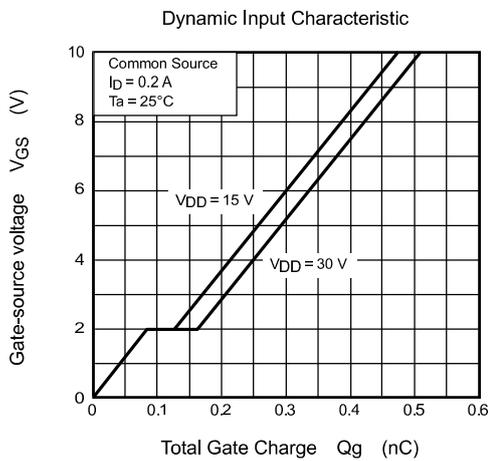
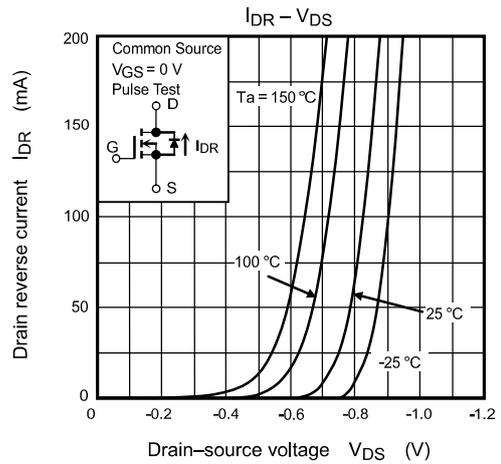
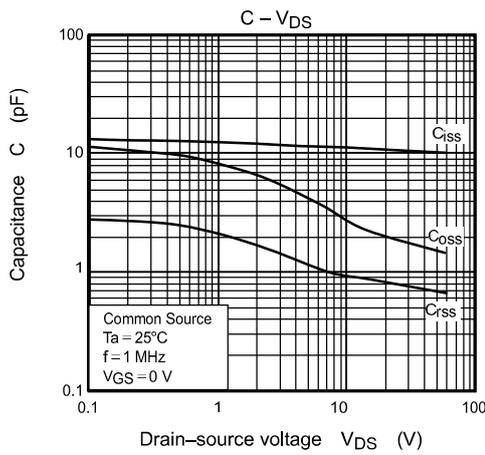
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (0.25 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th} , and $V_{GS(OFF)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.

Take this into consideration when using the device.

Handling Precaution

The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

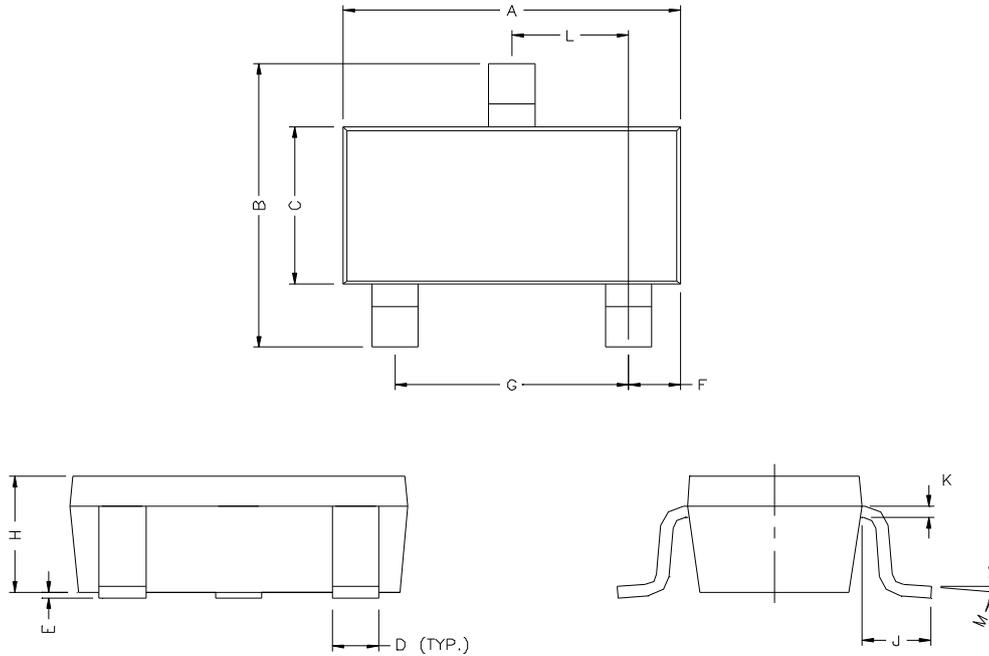




Note: The above characteristics curves are presented for reference only and not guaranteed by production test.

Package Outline

SOT23-3L



DIMENSIONS (mm are the original dimensions)

UNIT	A	B	C	D	E	F	G	H	K	J	L	M
mm	2.70 3.10	2.65 2.95	1.50 1.70	0.35 0.50	0 0.10	0.45 0.55	1.9	1.00 1.30	0.10 0.20	0.40 -	0.85 1.15	0° 10°

Summary of Packing Options

Package	Package Description	Packing Quantity	Industry Standard
SOT23-3L	Tape/Reel, 7" reel	3000	EIA-481-1