

650V N-CHANNEL ENHANCEMENT MODE MOSFET

MAIN CHARACTERISTICS

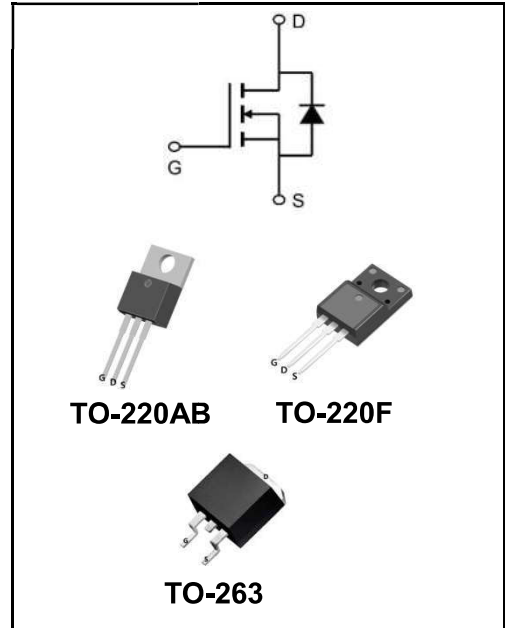
I_D	50A
V_{DSS}	650V(Type:740V)
R_{DS(on)-typ(@V_{GS}=10V)}	< 190mΩ(Type:150mΩ)

Features

◆Is CoolFET II MOSFET

Application

- ◆Uninterruptible Power Supply(UPS)
- ◆Power Factor Correction (PFC)



Product Specification Classification

Part Number	Package	Marking	Pack
YFWJ50N65AT	TO-220AB	YFW 50N65AT XXXXX	1000PCS/Box
YFWJ50N65AF	TO-220F	YFW 50N65AF XXXXX	1000PCS/Box
YFWJ50N65AS	TO-263	YFW 50N65AS XXXXX	800PCS/Tape

Maximum Ratings at T_c=25°C unless otherwise specified

Characteristics	Symbols	Value	Units
Drain-Source Voltage (V _{GS} = 0V)	V _{DS}	650	V
Continuous Drain Current	I _D	21	A
Pulsed Drain Current(note1)	I _{DM}	50	A
Gate - Source Voltage	V _{GS}	±30	V
Single Pulse Avalanche Energy(note2)	E _{AS}	500	mJ
Power Dissipation(T _c =25°C)	P _D	151	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C
Thermal Resistance, Junction-to-case	R _{θJC}	0.82	°C/W
Thermal Resistance, Junction ambient	R _{θJA}	62	°C/W

Maximum Ratings at Tc=25°C unless otherwise specified

Characteristics	Test Condition	Symbols	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	BV_{DSS}	650	740	-	V
Breakdown voltage temperature coefficient	Reference to 25°C, $I_D=250\mu A$	$\Delta BV_{DSS}/\Delta T_J$	-	0.7	-	V/°C
Drain -Source Leakage Current	$V_{DS}=650V, V_{GS}=0V$	I_{DSS}	-	-	1	μA
	$V_{DS}=520V, T_C=125^\circ C$		-	-	50	
Gate to source leakage current, forward	$V_{GS}=30V, V_{DS}=0V$	I_{GSS}	-	-	100	nA
Gate to source leakage current, reverse	$V_{GS}=-30V, V_{DS}=0V$		-	-	-100	
Gate- Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	$V_{GS(th)}$	2.5	3.3	4.5	V
Drain to source on state resistance	$V_{GS}=10V, I_D=3.2A$	$R_{DS(ON)}$	-	150	190	mΩ
Input Capacitance	$V_{DS}=100V$ $V_{GS}=0V$ $f=1MHz$	C_{iss}	-	1510	-	pF
Output Capacitance		C_{oss}	-	65	-	
Reverse Transfer Capacitance		C_{rss}	-	2.4	-	
Turn-on delay time	$V_{DS}=400V$ $I_D=13A$ $R_G=4.7\Omega$ $V_{GS}=13V$	$t_{d(on)}$	-	10	-	nS
Rising time		T_r	-	19.8	-	
Turn-Off Delay Time		$t_{d(OFF)}$	-	45.4	-	
Fall Time		t_f	-	41.4	-	
Total Gate Charge	$V_{DS}=480V$ $I_D=11A$ $V_{GS}=10V$	Q_g	-	7.27	-	nC
Gate-Source Charge		Q_{gs}	-	17.4	-	
Gate-Drain Charge		Q_{gd}	-	43.9	-	
Continuous source current	Integral reverse p-n Junction diode in the MOSFET	I_S	-	-	21	A
Pulsed source curren		I_{SM}	-	-	63	
Diode forward voltage drop	$I_S = 7.3A, V_{GS} = 0V$	V_{SD}	-	0.812	1.5	V
Reverse Recovery Time	$V_{GS} = 0V, I_S = 11A, V_{DD}=400V$ $diF/dt = 100A /\mu s$	t_{rr}	-	288	-	nS
Reverse Recovery Charge		Q_{rr}	-	3.66	-	uC

Note :

- 1、 The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . L=0.5mH, IAS =7A, VDD =50V, RG=25Ω
- 3、 The test condition is Pulse Test: $ISD \leq ID$, $di/dt = 100A/\mu s$, $VDD \leq BVDSS$, Starting at $T_J = 25^\circ C$
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

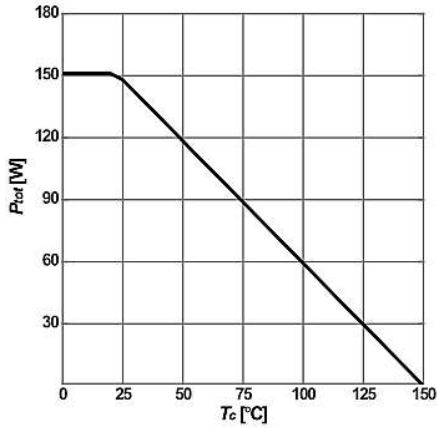


Figure1: Power dissipation (Non FullPAK)

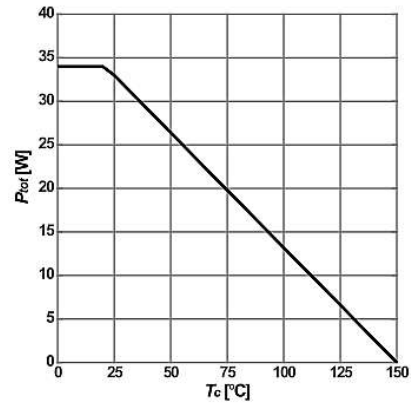


Figure2: Power dissipation (FullPAK)

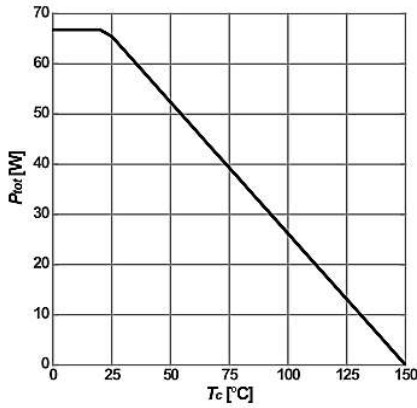


Figure3: Power dissipation
 $P_{tot}=f(T_c)$

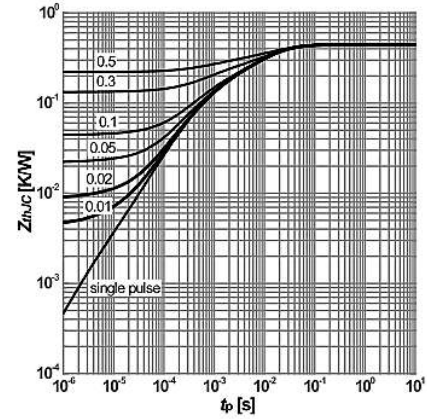


Figure4: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D= t_p/T$

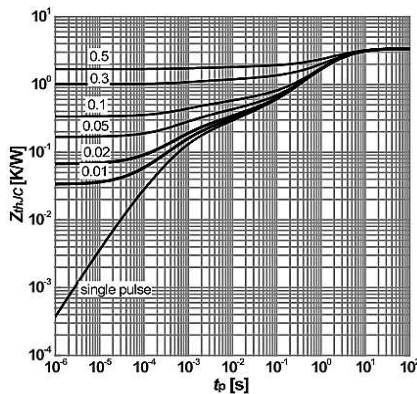


Figure5: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D= t_p/T$

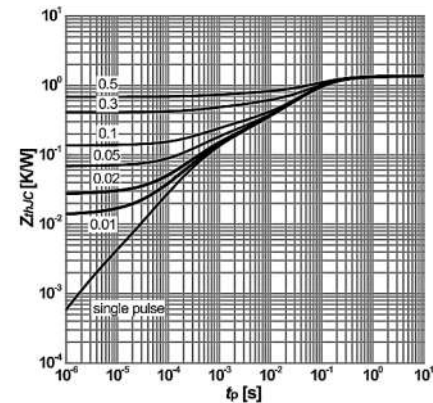


Figure6: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D= t_p/T$

Ratings and Characteristic Curves

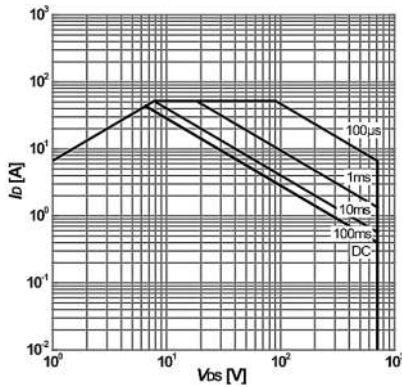


Figure 7: Safe operating area (Non FullPAK)
 $I_D=f(V_{DS}); T_J=25^\circ\text{C}; D=0$; parameter: t_p

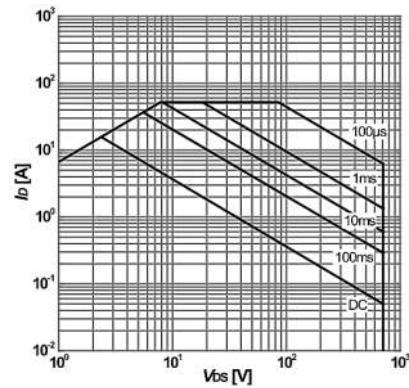


Figure 8: Safe operating area (Non FullPAK)
 $I_D=f(V_{DS}); T_J=25^\circ\text{C}; D=0$; parameter: t_p

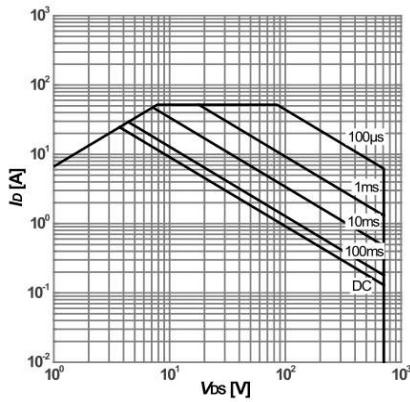


Figure 9: TSafe operating area (FullPAK-TO220A)
 $R_{DS(on)}=f(I_D); T_J=25^\circ\text{C}$; parameter: V_{GS}

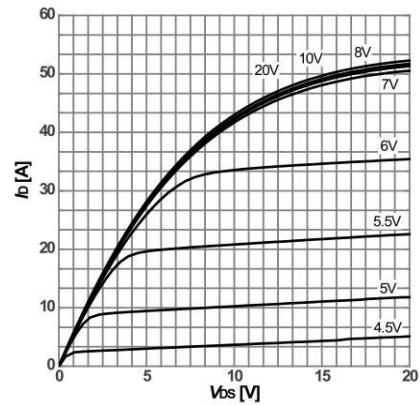


Figure 10: Typ. output characteristics
 $R_{DS(on)}=f(T_J); I_D=3.2\text{A}; V_{GS}=10\text{V}$

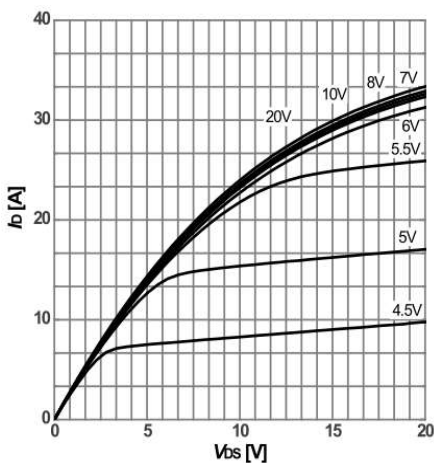


Figure 11: Typ. output characteristics
 $I_D=f(V_{DS}); T_J=125^\circ\text{C}$; parameter: V_{GS}

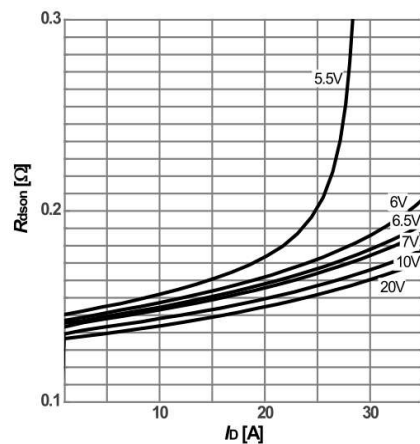


Figure 12: Type. gate charge
 $R_{DS(on)}=f(I_D); T_J=25^\circ\text{C}$; parameter: V_{GS}

Package Outline Dimensions Millimeters

TO-220AB

	Dim.	Min.	Max.
	A	10.15	10.35
	B	2.65	2.95
	C	3.70	3.90
	D	28.5	29.5
	E	1.30	1.45
	F	6.35	6.55
	G	2.9	3.3
	H	15.0	16.0
	I	0.38	0.42
	J	4.45	4.55
	K	1.25	1.35
	L	Typ 5.08	
	M	Typ 2.54	
N	3.1	3.3	
O	0.76	0.84	
All Dimensions in millimeter			

TO-220F

	Dim.	Min.	Max.
	A	9.95	10.25
	B	2.95	3.25
	C	1.25	1.45
	D	12.95	13.25
	E	0.50	0.65
	F	3.1	3.3
	G	1.30	1.45
	H	Typ 2.54	
	I	Typ 5.08	
	J	4.60	4.75
	K	2.50	2.65
	L	6.35	6.55
	M	15.4	16.0
	N	2.75	3.05
	O	0.48	0.52
P	0.76	0.84	
All Dimensions in millimeter			

Package Outline Dimensions Millimeters

TO-263

Dim.	Min.	Max.
A	10.1	10.2
B	7.4	7.6
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.78	0.86
H	1.2	1.3
I	Typ2.54	
J	8.4	8.6
K	4.45	4.55
L	1.25	1.35
M	0.02	0.1
N	2.4	2.8
O	0.36	0.40
All Dimensions in millimeter		