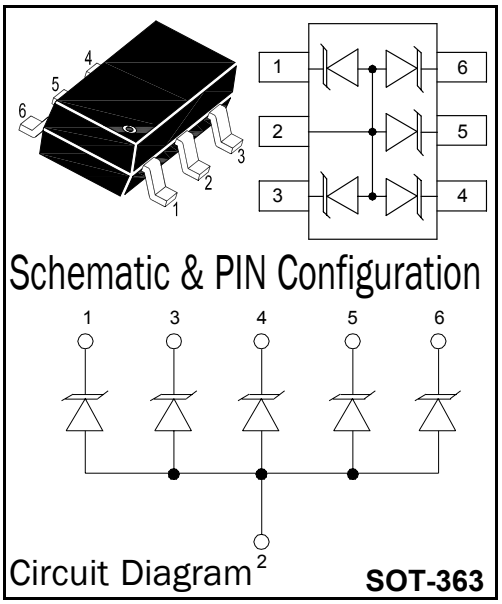
Tvs Diode Array For ESD and Latch-Up Protection

Features

- ESD protection for data lines to
  IEC 61000-4-2(ESD)+15kV(air),± 8kV(contact)
  IEC61000-4-4(EFT) 40A (5/50ns)
- Small package for use in portable electronics
- Protects five I/o lines
- Working voltage: 5V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon-avalanche technology



Application

- Cellular Handsets and Accessories
- Cordless Phones
- Personal Digital Assistants (PDA's)
- Notebooks and Handhelds
- Portable Instrumentation
- Digital Cameras
- Peripherals
- MP3 Players

Order Information

Part Number	Package	Marking	Size (mm)	Delivery Form	Delivery Quantity
SMF05C	SOT-363	5C	2.0X2.1X0.95	7" T&R	3000PCS/Tape

Absolute Maximum Ratings Ta= 25℃

Symbol	Parameter	Conditions	value	Unit
P_{Pk}	Peak Pulse Power	tP = 8/20 μs	100	W
I_{PP}	Peak Pulse Current	tP = 8/20 μs	8	A
V_{ESD}	ESD per IEC 61000-4-2 ESD per IEC 61000-4-2	Air Contact	20 15	KV
T_L	Lead Soldering Temperature	-	260(10seconds)	V
T_J	Operating Temperature	-	-55 to+125	℃
Tstg	Storage Temperature Range	-	-55 to+150	℃

Electrical Characteristics Ta = 25℃

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse Stand-Off Voltage		-	-	5	V
V_{BR}	Reverse Breakdown Voltage	IT = 1mA	6	-	-	V
I_R	Reverse Leakage Current	V_{RWM} = 36 V; T = 25 °C	-	-	5	uA
V_C	Clamping Voltage	IPP=5 A, tP =8/20μs	-	-	9.8	V
V_C	Clamping Voltage	IPP=8 A, tP =8/20μs	-	-	12.5	V
CJ	Junction Capacitance	VR = 0V, f = 1 MHz	-	-	130	pF

Typical Characteristics

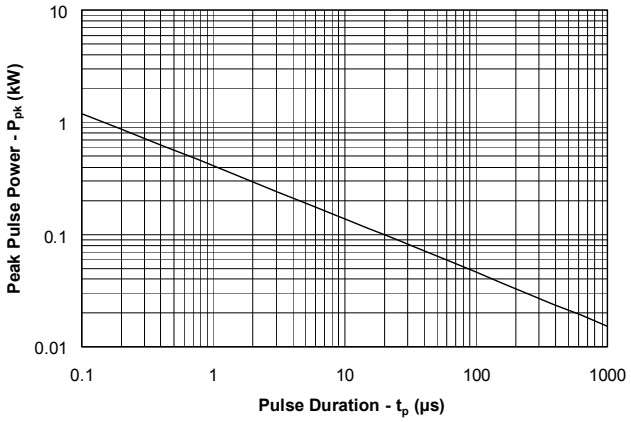


Fig.1 Non-Repetitive Peak Pulse Power vs. Pulse Time

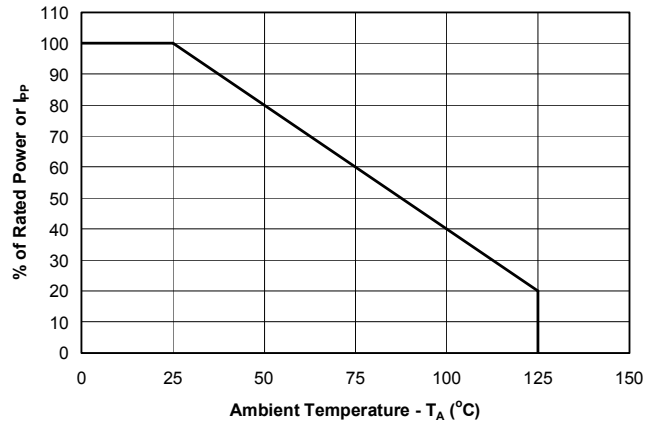


Fig.2 Power Derating Curve

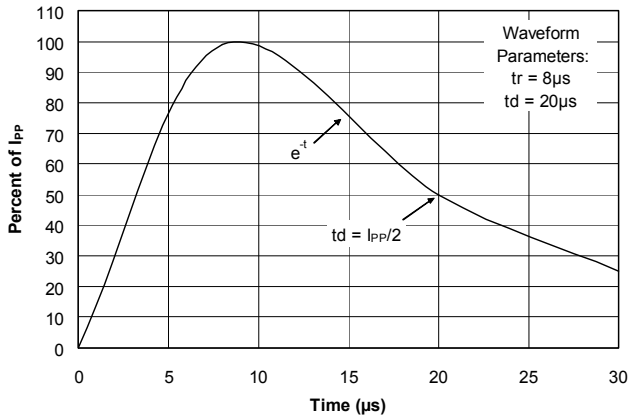


Fig.3 Pulse Waveform

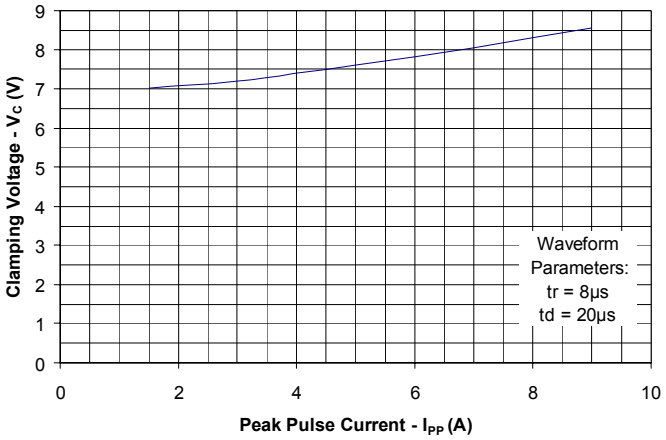


Fig. 4 Clamping Voltage vs. Peak Pulse Current

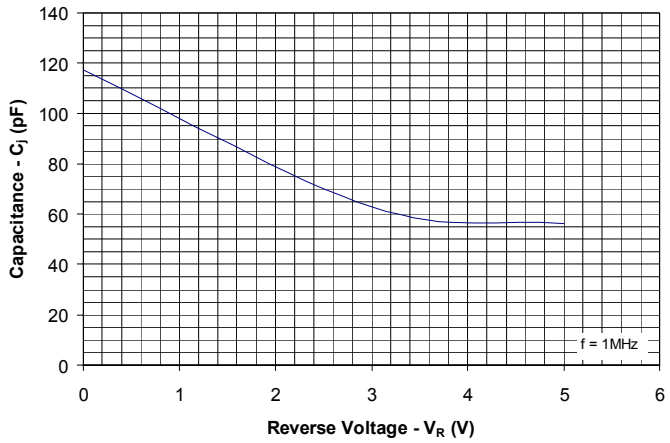


Fig. 5 Capacitance vs.Reverse Voltage

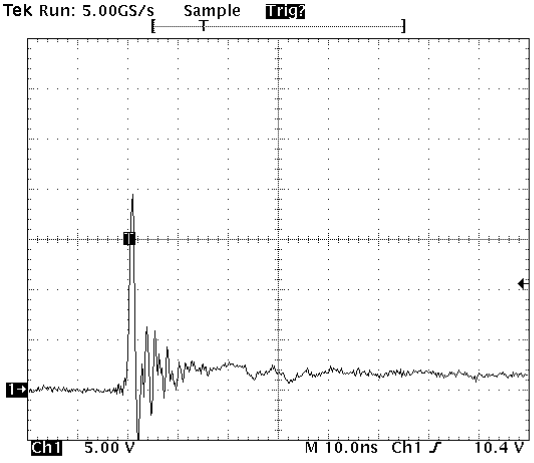


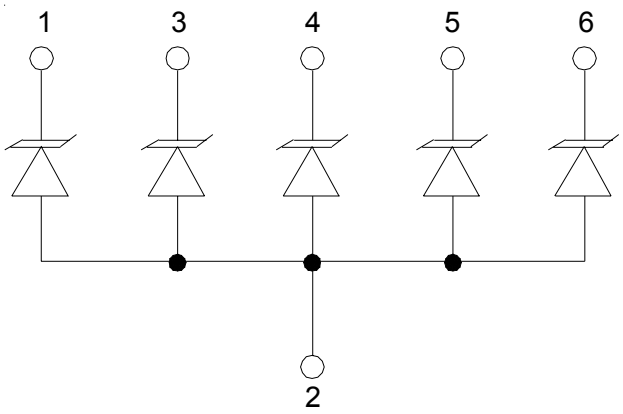
Fig. 6 ESD Clamping Characteristics (8kV Contact Discharge per IEC 61000-4-2)

Device Connection for Protection of Five Data Lines

The SMF05C is designed to protect up to five unidirec-tional data lines.
The device is connected as follows:

1, Unidirectional protection of five I/o lines is achieved by connecting pins 1,3, 4,5 and 6 to thedata lines. Pin 2 is connected to ground. Theground connection should be made directly to theground plane for best results. The path length iskept as short as possible to reduce the effects ofparasitic inductance in the board traces.

SMF05C Circuit Diagram

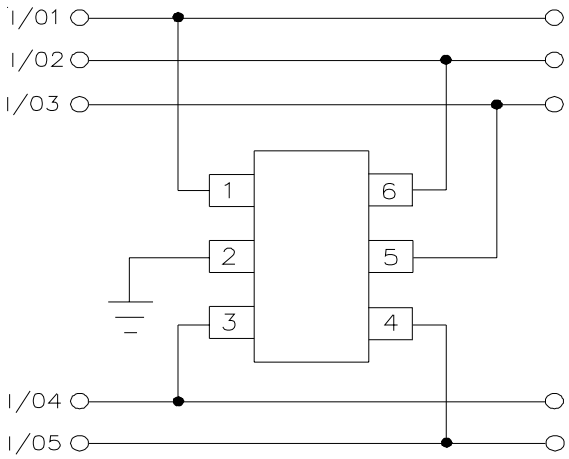


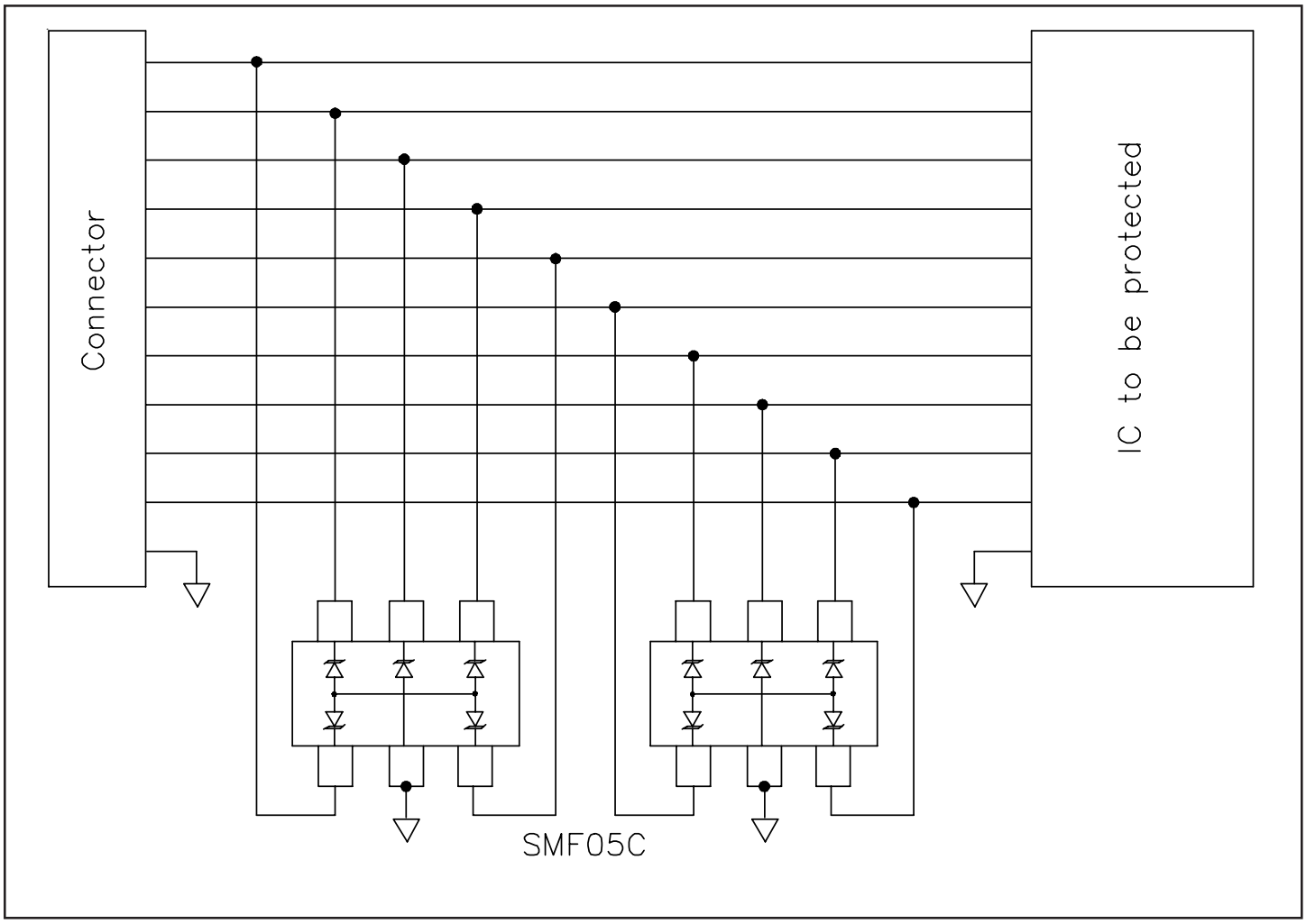
Circuit Board Layout Recommendations for Suppres-sion of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

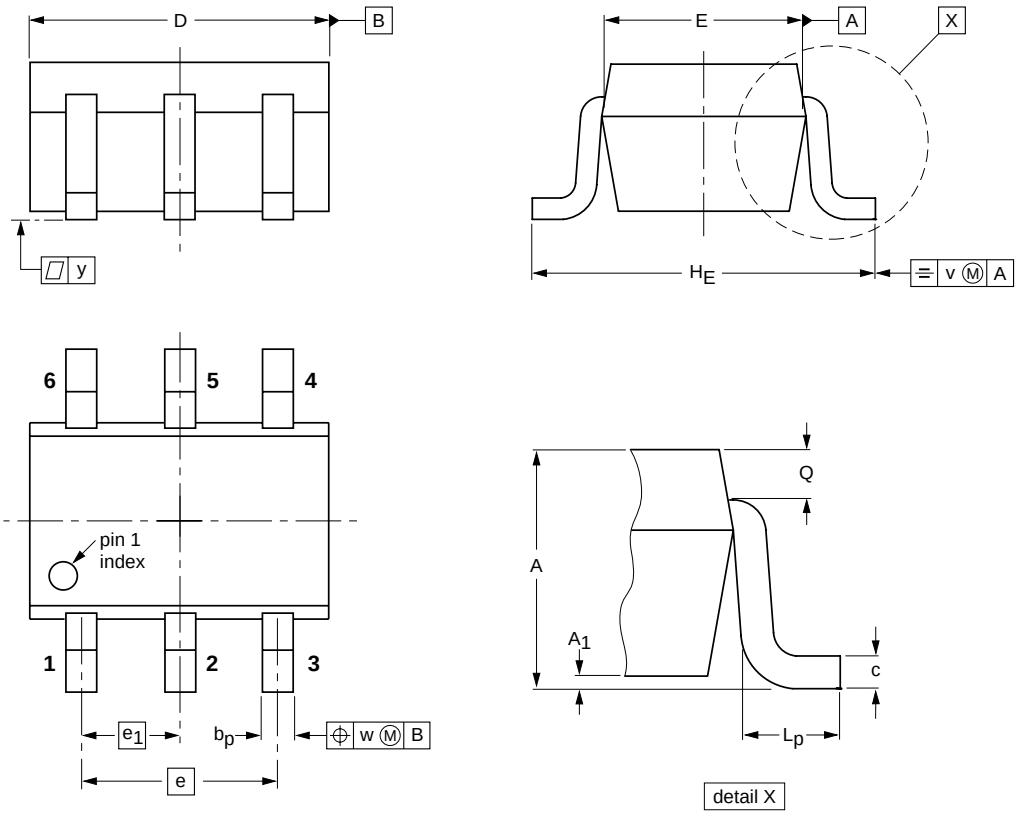
1.Place the SMF05C near the input terminals or connectors to restrict transient coupling.
2.Minimize the path length between the SMF05C an the protected line.
3.Minimize all conductive loops including power and ground loops.
4.The ESD transient return path to ground should be kept as short as possible.
5.Never run critical signals near board edges.
6.Use ground planes whenever possible.

Protection of Five Unidirectional Lines




Connector
IC to be protected
SMF05C

Package Outline SOT-363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

Summary of Packing Options

Package	Package Description	Packing Quantity	Industry Standard
SOT-363	Tape/Reel,7"reel	3000	EIA-481-1