

300mA Low-Dropout Linear Regulators

Features

- V_{IN} Range: 2.5V ~ 6V
- V_{OUT} Range: 0.8V ~ 5.0V $\pm 1\%$ ($\pm 20mV$)
- 3-Kind of SET Voltages: 0.8V, 1.0V, 1.2V $\pm 1\%$
- Maximum I_{OUT} Rated: 300mA
- Dropout Voltage: 210mV @ $I_{OUT} = 0.3A$, $V_{OUT} = 3.3V$
- 60 μA No-Load Supply Current
- Stable with Ceramic Capacitors
- Output Discharge for Fast Turn-Off
- Over-Temperature Protection
- Short-Circuit Protection

Applications

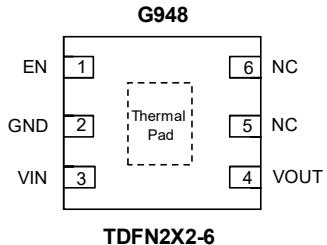
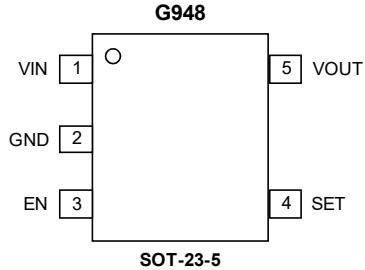
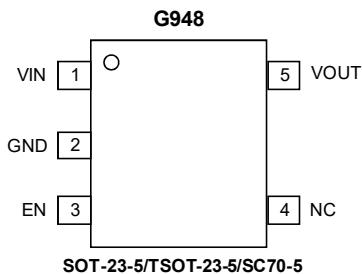
- Notebook Computers
- Portable Devices
- Hand-Held Devices

General Description

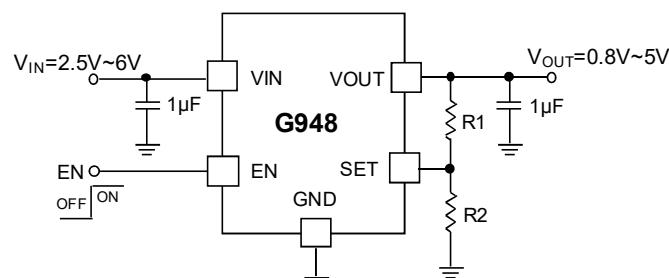
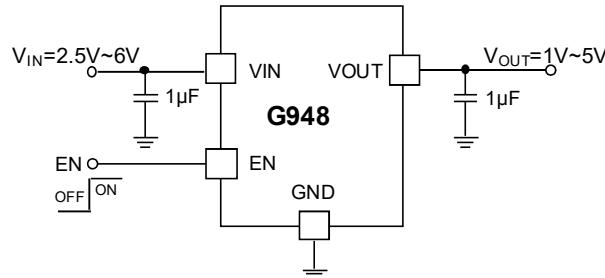
The G948 is a low-supply current, low-dropout linear regulator. An over-temperature protection circuit is built-in in the G948 to prevent thermal overload. These power-saving features make the G948 ideal for use in a battery-powered application such as notebook computers, and portable devices.

These devices feature a shutdown function and are offered in active low with auto discharge. The G948 is specifically designed for ceramic output capacitors. The G948 comes in a space-saving SOT-23-5, TSOT23-5, SC70-5 and TDFN2x2-6 packages

Pin Configuration



Typical Application Circuit



Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Ordering Information

ORDER NUMBER	MARKING	VOUT (V)	IOUT (A)	PACKAGE (Green)
G948C3120T11G	98AAx	1.20	0.3	SOT-23-5
G948C3150T11G	98ABx	1.50	0.3	SOT-23-5
G948C3180T11G	98ACx	1.80	0.3	SOT-23-5
G948C3250T11G	98ADx	2.50	0.3	SOT-23-5
G948C3280T11G	98AE _x	2.80	0.3	SOT-23-5
G948C3300T11G	98AF _x	3.00	0.3	SOT-23-5
G948C3330T11G	98AGx	3.30	0.3	SOT-23-5
G948C3A08T11G	98AHx	$V_{SET} = 0.8V$	0.3	SOT-23-5
G948C3A10T11G	98AIx	$V_{SET} = 1.0V$	0.3	SOT-23-5
G948C3A12T11G	98AJx	$V_{SET} = 1.2V$	0.3	SOT-23-5
G948C3180TO1G	98ACx	1.80	0.3	TSOT-23-5
G948C3330TO1G	98AGx	3.30	0.3	TSOT-23-5
G948C3180TA1G	9ACx	1.80	0.3	SC70-5
G948C3250TA1G	9ADx	2.50	0.3	SC70-5
G948C3330TA1G	9AGx	3.30	0.3	SC70-5
G948C3180RB1U	98AC	1.80	0.3	TDFN2x2-6
G948C3330RB1U	98AG	3.30	0.3	TDFN2x2-6

G948①②③④⑤

⑤ Pin 1 Orientation in Taping

U: Upper left

G: Lower left

④ Bonding Code: 1

③ Package code & bonding Code

TA : SC70-5

T1 : SOT-23-5

TO : TSOT-23-5

RB : TDFN2x2-6

② Output voltage

A 3-digital number from 100 to 500 steps every 5,

Fixed output voltage from 1.00V to 5.00V, steps every 0.05V

A08 : Adjustable output voltage, $V_{SET} = 0.8V$

A10 : Adjustable output voltage, $V_{SET} = 1.0V$

A12 : Adjustable output voltage, $V_{SET} = 1.2V$

① Output Current capability

C3 : 0.3Ampere output current

Absolute Maximum Ratings

V_{IN} to GND -0.3V to +6.5V
 V_{OUT} to GND -0.3V to (V_{IN} + 0.3V)
 EN to GND -0.3V to (V_{IN} + 0.3V)

Operating Temperature Range -40°C to +85°C
 Junction Temperature 150°C
 Storage Temperature Range -55°C to +150°C
 Reflow Temperature (soldering, 10sec) 260°C

Recommendation operation conditions

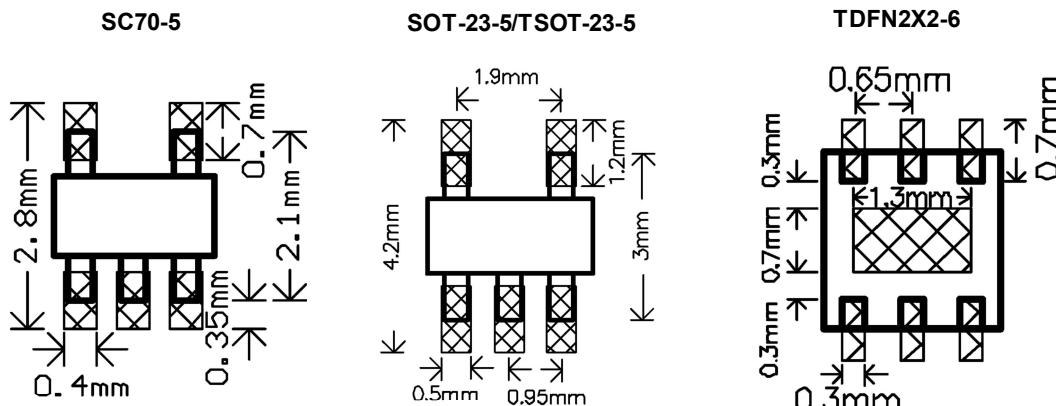
THERMAL METRIC		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	2.5	---	6.0	V
V_{OUT}	Output voltage	0.8	---	5.0	V
V_{EN}	Enable Voltage	0	---	V_{IN}	V
I_{OUT}	Output current	0	---	0.3	A
C_{IN}	Input capacitance, X7R MLCC or low ESR cap	1	---	---	μ F
C_{OUT}	Output capacitance, X7R MLCC	1	---	10	μ F

Thermal Information

THERMAL METRIC		TDFN2x2-6	SC70-5	SOT-23-5	TSOT-23-5	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	88.2	210.7	191.0	194.3	°C/W
$R_{\theta JC_top}$	Junction to case top thermal resistance	143.4	134.4	130.0	81.0	°C/W
$R_{\theta JB}$	Junction to board thermal resistance	50.5	63.0	61.0	57.3	°C/W
Ψ_{JT}	Junction to top characterization parameter	10.3	29.3	32.3	26.7	°C/W
Ψ_{JB}	Junction to board characterization parameter	50.5	63.0	61.0	57.0	°C/W
$R_{\theta JC_bot}$	Junction to case bottom thermal resistance	24.8	N/A	N/A	N/A	°C/W

1. Package thermal metric is obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
2. The maximum power dissipation is $P_{D(MAX)} = \frac{(T_{JMAX} - T_A)}{R_{\theta JA}}$, Exceeding the maximum allowable power dissipation results in excessive die temperature, and the device will enter thermal shutdown.

Minimum Footprint PCB Layout Section



Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, $V_{IN} \geq 2.5V$, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = T_J = +25^\circ C$)⁽¹⁾

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	
Input Voltage ⁽¹⁾	V_{IN}		2.5	---	6	V	
Quiescent Current	I_Q	$I_{OUT} = 0mA$	---	60	---	μA	
Shutdown Current	I_{SDN}	$V_{EN} \leq 0.4V, V_{IN} = 5.5V$	---	---	0.5	μA	
Output Voltage Accuracy	V_{OUT}	$I_{OUT} = 1mA$	x0.99 $V_{OUT} > 2V$ $V_{OUT} \leq 2V$	-20	---	+20	mV
SET Reference Voltage ⁽²⁾	V_{SET}	$V_{IN} = 2.5V$ to $5.5V$, $I_{OUT} = 1mA$	1.176 0.990 0.792	1.2 1.0 0.8	1.224 1.010 0.808	V	
SET Input Leakage Current	I_{SET}	$V_{SET} = 1.3V$	---	5	30	nA	
Dropout Voltage ⁽³⁾	V_{DO}	$I_{OUT} = 300mA$	2.5V $\leq V_{OUT} < 2.8V$ 2.8V $\leq V_{OUT} < 3.3V$ $V_{OUT} \leq 3.3V$	360 270 210	560 410 320	mV	
Output Current Limit	I_{LIMIT}	$V_{OUT} = 90\% * V_{OUT(NOM)}$ $V_{IN} = V_{OUT} + 1V$, $V_{IN} = 3V$ for $V_{OUT} \leq 2.0V$	400	500	---	mA	
Line Regulation ⁽⁴⁾	V_{LNR}	$I_{OUT} = 1mA$, $V_{OUT} + 0.5V < V_{IN} < 5.0V$ $V_{IN} = 2.5V$ for $V_{OUT} \leq 2.0V$	---	0.3	---	%/V	
Load Regulation	V_{LDR}	$I_{OUT} = 1mA$ to $300mA$ $V_{IN} = \max(V_{OUT} + 1V, 2.5V)$ $V_{IN} = 3V$ for $V_{OUT} \leq 2.0V$	---	0.5	1	%	
Power Supply Rejection Ratio	PSRR	$F = 100Hz$, Ripple $0.2Vp-p$, $V_{OUT} = V_{IN} + 1V$, $I_{OUT} = 30mA$ $V_{IN} = 3V$ for $V_{OUT} \leq 2.0V$	---	65	---	dB	
Output Noise Voltage	en	$I_{OUT} = 30mA$, $F = 10Hz$ to $100kHz$	---	60	---	μV_{RMS}	
Enable Input Threshold	V_{EN_HI} V_{EN_LO}		1 ---	---	0.4	V	
Enable Pin Input Resistance	R_{EN}	$V_{OUT} = 3.3V$	---	2	---	$M\Omega$	
Discharge Resistance	R_{DIS}	$V_{EN} \leq 0.4V$, $V_{IN} = 5.5V$	---	100	---	Ω	
Thermal Shutdown Temperature	T_{SHDN}		---	150	---	$^\circ C$	
Thermal Shutdown Hysteresis	ΔT_{SHDN}		---	20	---	$^\circ C$	

Note 1: Limits is 100% production tested at $T_A = +25^\circ C$. Low-duty pulse techniques are used during the test to maintain junction temperature as close to ambient as possible.

Note 2: SET only exists at V_{OUT} Adjustable mode.

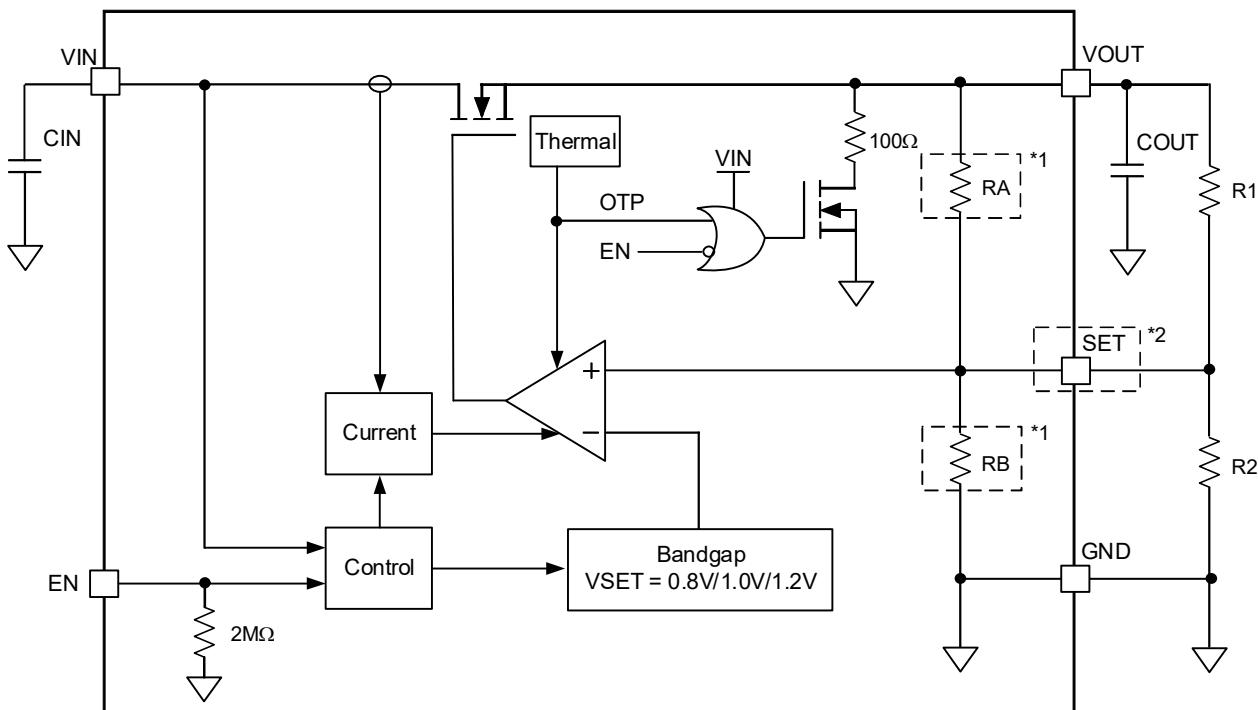
Note 3: The dropout voltage is defined as $(V_{IN} - V_{OUT})$ when V_{OUT} drops $100mV$ below the regulated output voltage $V_{OUT(NOM)}$ at $V_{IN} = \text{maximum}(V_{OUT(NOM)} + 0.3V \text{ or } 2.5V)$

Note 4: $V_{LNR}(\%V) = \frac{(V_{OUT@V_{IN}=5V} - V_{OUT@V_{IN}=V_{OUT}+0.5V})}{V_{OUT@V_{IN}=V_{OUT}+0.5V} \times (4.5V - V_{OUT})}$

Pin Description

PIN			NAME	FUNCTION
SOT-23-5/ TSOT-23-5/ SC70-5	SOT-23-5	TDFN2x2-6		
5	5	4	VOUT	The power output of the device.
2	2	2	GND	Reference ground.
3	3	1	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value.
1	1	3	VIN	Input voltage. Large bulk capacitance should be placed close to this pin. A 1μF ceramic capacitor is recommended at this pin.
---	4	---	SET	Feedback Input for Setting the Output Voltage. Connect to an external resistor divider for adjustable-output operation.
4	---	5.6	NC	No Connection

Block Diagram



Note

*1: The internal dividing resistors of RA and RB only exist in fixed output mode.

*2: The SET pin only exists in adjustable output mode and both the internal RA and RB don't exist.

*3: R2 of 100KΩ is recommended

Application

Capacitor Selection and Regulator Stability

$1\mu\text{F}$ capacitor on the input and a $1\mu\text{F}$ capacitor on the output of the G948. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Larger input capacitance and lower ESR provide better supply-noise rejection and transient response; An appropriate output capacitance helps ensure stability and improve dynamic performance. A large input or output capacitance may be necessarily located near G948 for anticipated large fast transient loads causing a drop voltage on V_{IN} or V_{OUT} .

EN and power sequence

EN has a pull low resistance of $2M\Omega$ for avoiding the EN at floating unknown status. G948 is enabled if $V_{EN} > V_{EN_HI}$, and G948 is disabled if $V_{EN} > V_{EN_LO}$. If power sequence control of the V_{OUT} is not needed, connect EN pin to VIN pin. V_{IN} comes before E_{EN} and V_{IN} falls after V_{EN} in typically power sequence control.

Output Voltage

G948 has two types of ways to set the output voltage. The fixed output voltage, V_{OUT} range is from 1.0V to 5.0V steps every 0.05V. For the adjustable type, its V_{SET} has three kinds of voltage 0.8V, 1.0V, and 1.2V. The G948 allows the V_{OUT} to be adjusted by two external resistors connected between the VOUT pin and GND pin. The V_{OUT} can be calculated by Equation 1, The R_2 of $100\text{K}\Omega$ is recommended.

Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current; where the internal MOSFET is fully on in operation, which acts the V_{IN} to V_{OUT} as the drain-source on-state resistance RDS_{ON} . The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed V_{OUT} which is expected to stay in regulation at the rated output current. If the V_{IN} keeps falling to less than the value required to maintain V_{OUT} regulation, then the V_{OUT} falls as well. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly.

V_{OUT} Discharge

G948 is disabled or Over-temperature Protection occurs. The VOUT discharge function is active. The discharge function provides an internal discharge path of 100Ω between VOUT and GND.

Line Regulation

Line regulation is the ability of G948 to maintain a constant V_{OUT} or current despite changes in the input voltage or power supply. In other words, it measures how well G948 can maintain a stable V_{OUT} over a range of input voltages. Its formula is defined as

$$V_{LNR}(\% / V) = \frac{V_{OUT@VIN=5V} - V_{OUT@VIN=VOUT+0.5V}}{V_{OUT@VIN=VOUT+0.5V} \times (4.5V - V_{OUT})} \times 100\% .$$

(2)

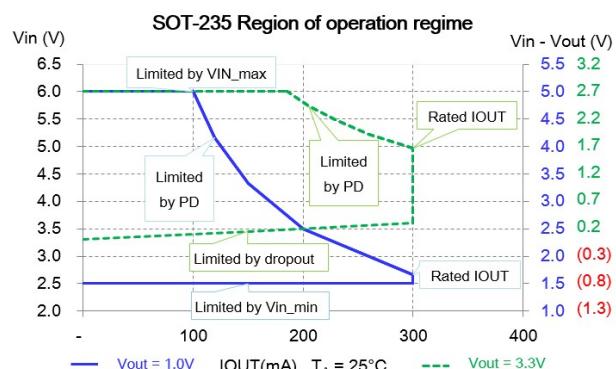
Load Regulation

Load regulation is a power supply's ability to maintain the specified V_{OUT} under varying load conditions. The worst case of V_{OUT} variations occurs as the load current transitions from 0A to its maximum rated current. Load regulation is defined as formula 3.

$$V_{LDR}(\%) = \frac{V_{OUT@I_{OUT}=0A} - V_{OUT@I_{OUT}=\text{Rated current}}}{V_{OUT@I_{OUT}=\text{Rated current}}} \times 100\% \quad (3)$$

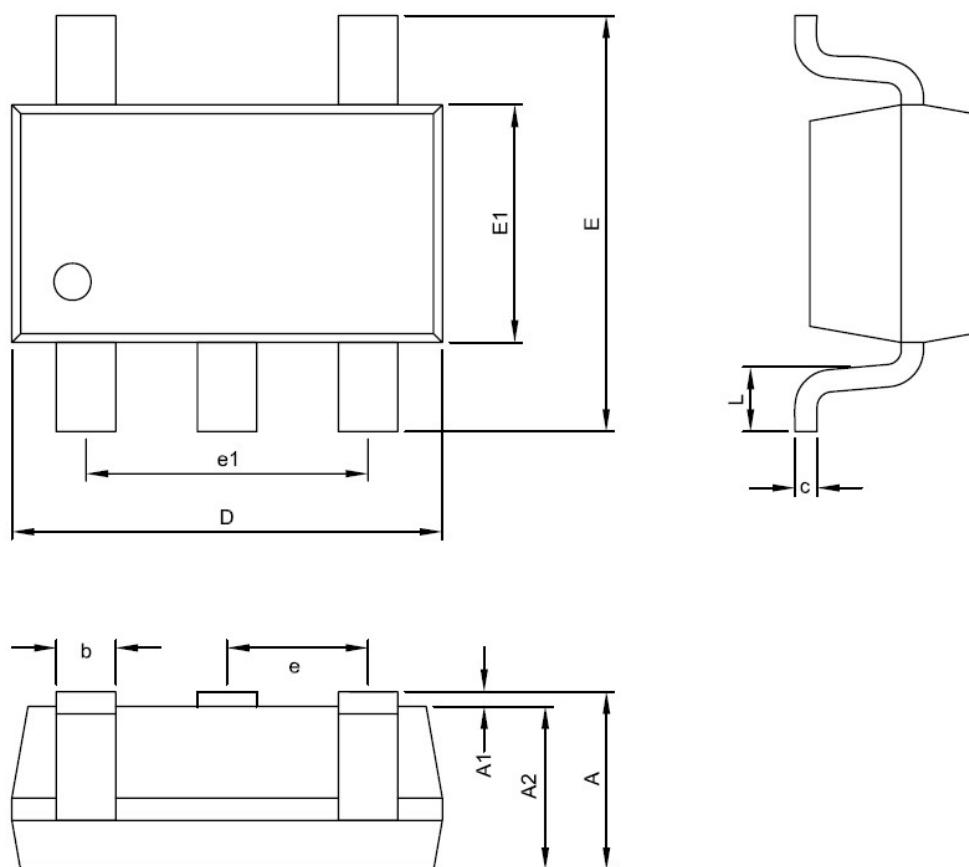
Power Dissipation and Operation Regime

The maximum power dissipation for which the regulator will operate within specifications. G948 I_{OUT} operation regime is limited by dropout or V_{IN}, Rated current, or power dissipation of packages.

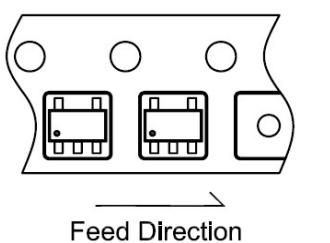


Over Temperature Protection

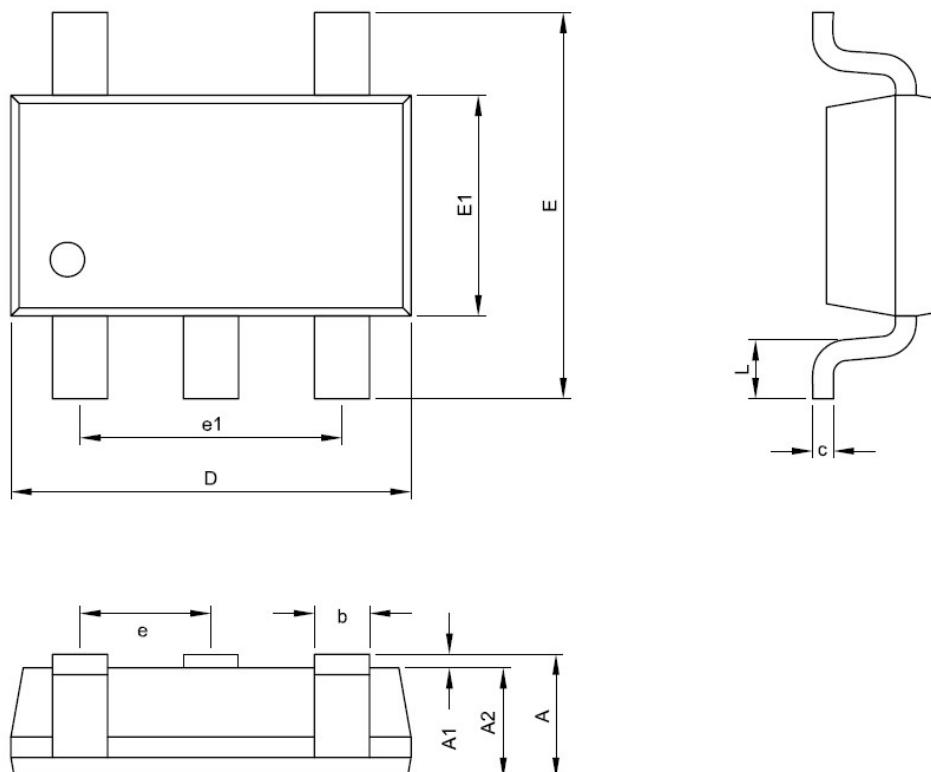
The G948 has a built-in temperature monitoring circuit. When the junction temperature is above 150°C, G948 is turned off. When the silicon is cooling down to below 130°C, the output is turned on again.

Package Information

SOT-23-5 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.10	1.45	0.037	0.043	0.057
A1	0.00	---	0.15	0.000	---	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

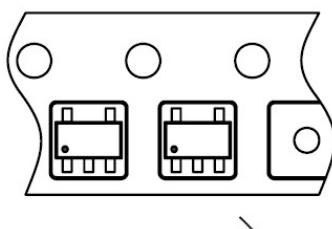
Taping Specification


PACKAGE	Q'TY/REEL
SOT-23-5	3,000 ea

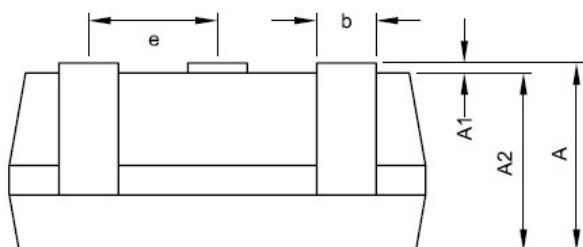
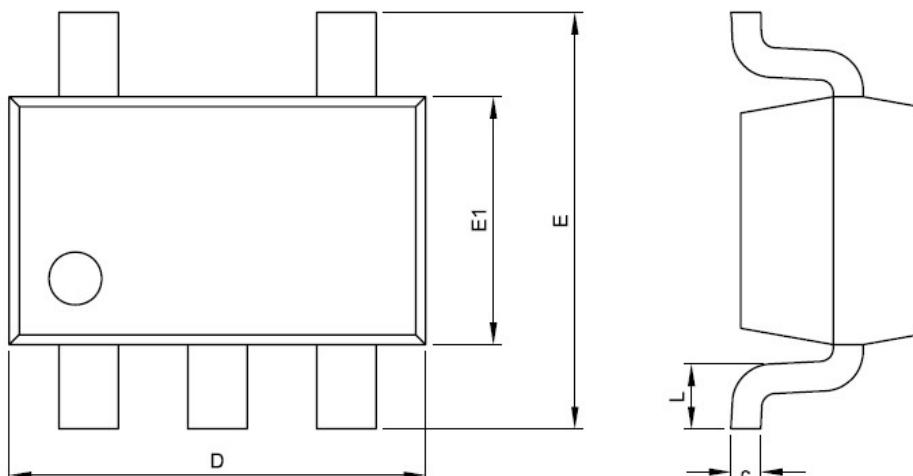

TSOT-23-5 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70	0.75	0.80	0.028	0.030	0.031
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.15 REF			0.006 REF		
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Taping Specification

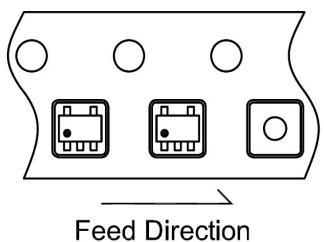


PACKAGE	Q'TY/REEL
TSOT-23-5	3,000 ea

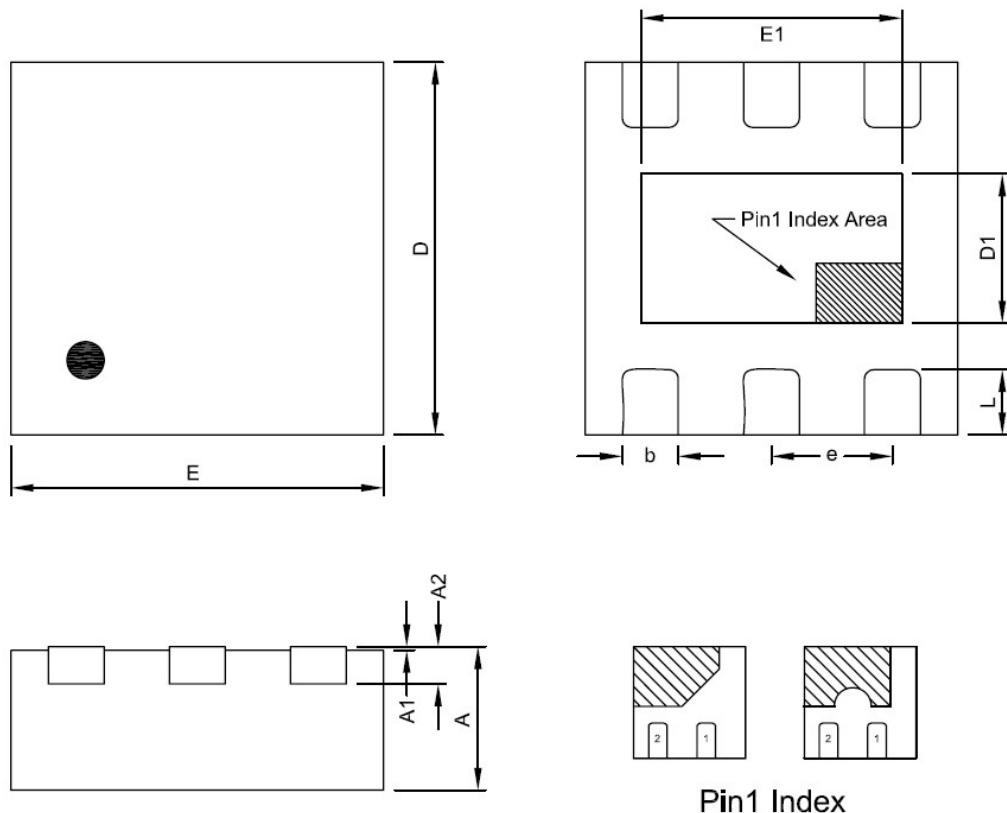

SC70-5 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.028	0.035	0.039
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.45	0.071	0.083	0.096
E1	1.15	1.25	1.35	0.045	0.049	0.053
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.15	0.25	0.40	0.006	0.010	0.016
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018

Taping Specification

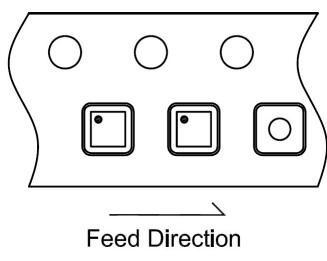


PACKAGE	Q'TY/REEL
SC70-5	3,000 ea


TDFN2X2-6 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF				0.0079 REF	
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.55	0.70	0.85	0.0217	0.0276	0.0335
E1	1.15	1.30	1.45	0.0453	0.0512	0.0571
b	0.20	0.30	0.35	0.0079	0.0118	0.0138
e	0.65 BSC				0.0256 BSC	
L	0.30	0.35	0.40	0.0118	0.0138	0.0157

Taping Specification



PACKAGE	Q'TY/REEL
TDFN2X2-6	3,000 ea

GMT Inc. does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and GMT Inc. reserves the right at any time without notice to change said circuitry and specifications.