

74HC165; 74HCT165

8-bit parallel-in/serial out shift register

Rev. 5 — 21 August 2017

Product data sheet

1 General description

The 74HC165; 74HCT165 are 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input (\overline{PL}) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When \overline{PL} is HIGH data enters the register serially at DS. When the clock enable input (\overline{CE}) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on \overline{CE} will disable the CP input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2 Features and benefits

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Complies with JEDEC standard no. 7A
- Input levels:
 - For 74HC165: CMOS level
 - For 74HCT165: TTL level
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3 Applications

- Parallel-to-serial data conversion

4 Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------|----------|
| | Temperature range | Name | Description | |
| 74HC165D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT165D | | | | |
| 74HC165DB | -40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT165DB | | | | |
| 74HC165PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT165PW | | | | |
| 74HC165BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74HCT165BQ | | | | |

5 Functional diagram

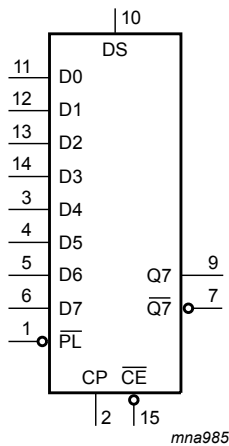


Figure 1. Logic symbol

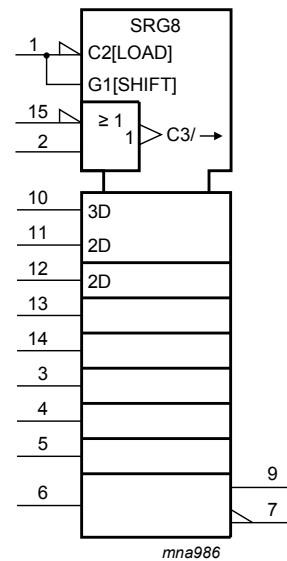


Figure 2. IEC logic symbol

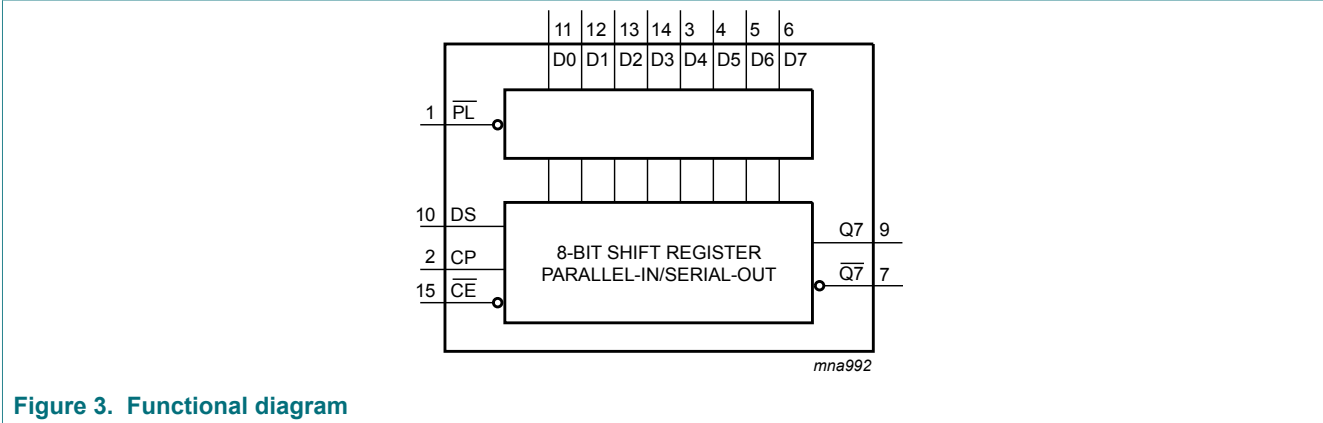


Figure 3. Functional diagram

6 Pinning information

6.1 Pinning

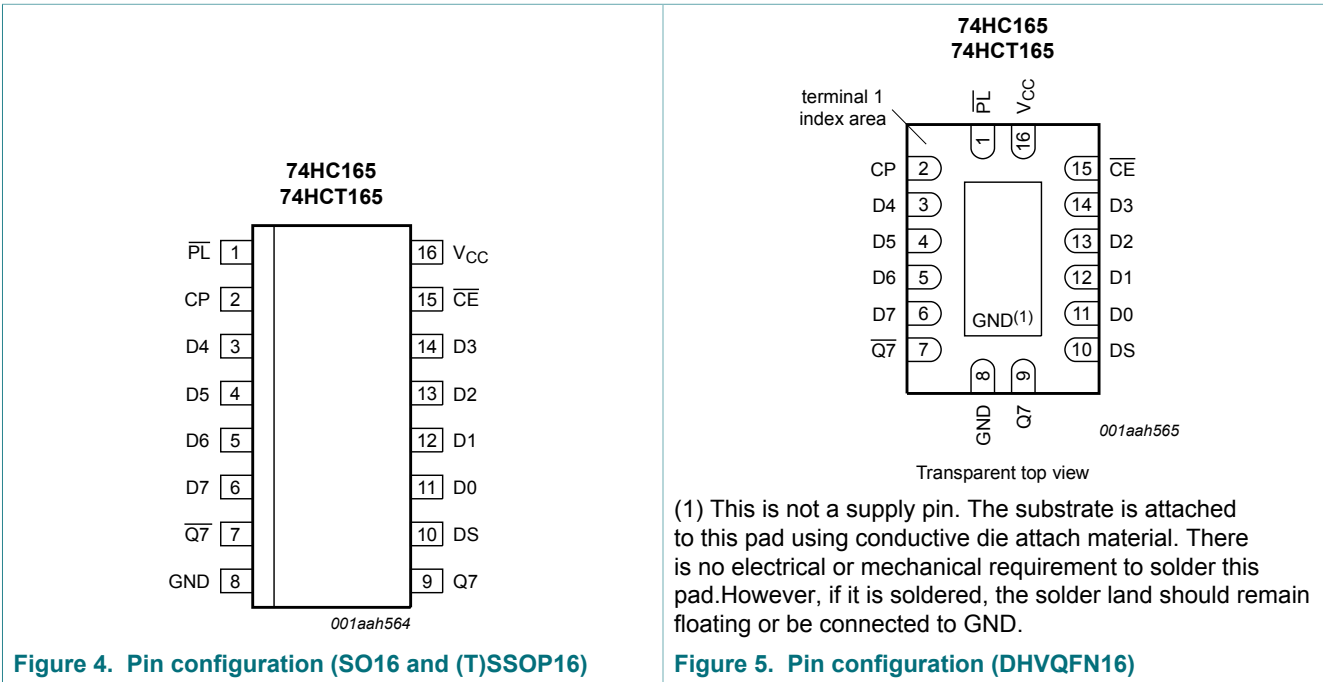


Figure 4. Pin configuration (SO16 and (T)SSOP16)

Figure 5. Pin configuration (DHVQFN16)

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------------|----------------------------|-----------------------------------------------|
| $\overline{\text{PL}}$ | 1 | asynchronous parallel load input (active LOW) |
| CP | 2 | clock input (LOW-to-HIGH edge-triggered) |
| $\overline{\text{Q7}}$ | 7 | complementary output from the last stage |
| GND | 8 | ground (0 V) |
| Q7 | 9 | serial output from the last stage |
| DS | 10 | serial data input |
| D0 to D7 | 11, 12, 13, 14, 3, 4, 5, 6 | parallel data inputs (also referred to as Dn) |
| $\overline{\text{CE}}$ | 15 | clock enable input (active LOW) |
| V _{CC} | 16 | positive supply voltage |

7 Functional description

Table 3. Function table ^[1]

| Operating modes | Inputs | | | | | Qn registers | | Outputs | |
|-------------------|------------------------|------------------------|----|----|----------|--------------|----------|---------|------------------------|
| | $\overline{\text{PL}}$ | $\overline{\text{CE}}$ | CP | DS | D0 to D7 | Q0 | Q1 to Q6 | Q7 | $\overline{\text{Q7}}$ |
| parallel load | L | X | X | X | L | L | L to L | L | H |
| | L | X | X | X | H | H | H to H | H | L |
| serial shift | H | L | ↑ | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | L | ↑ | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | l | X | L | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| | H | ↑ | L | h | X | H | q0 to q5 | q6 | $\overline{\text{q6}}$ |
| hold "do nothing" | H | H | X | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |
| | H | X | H | X | X | q0 | q1 to q6 | q7 | $\overline{\text{q7}}$ |

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

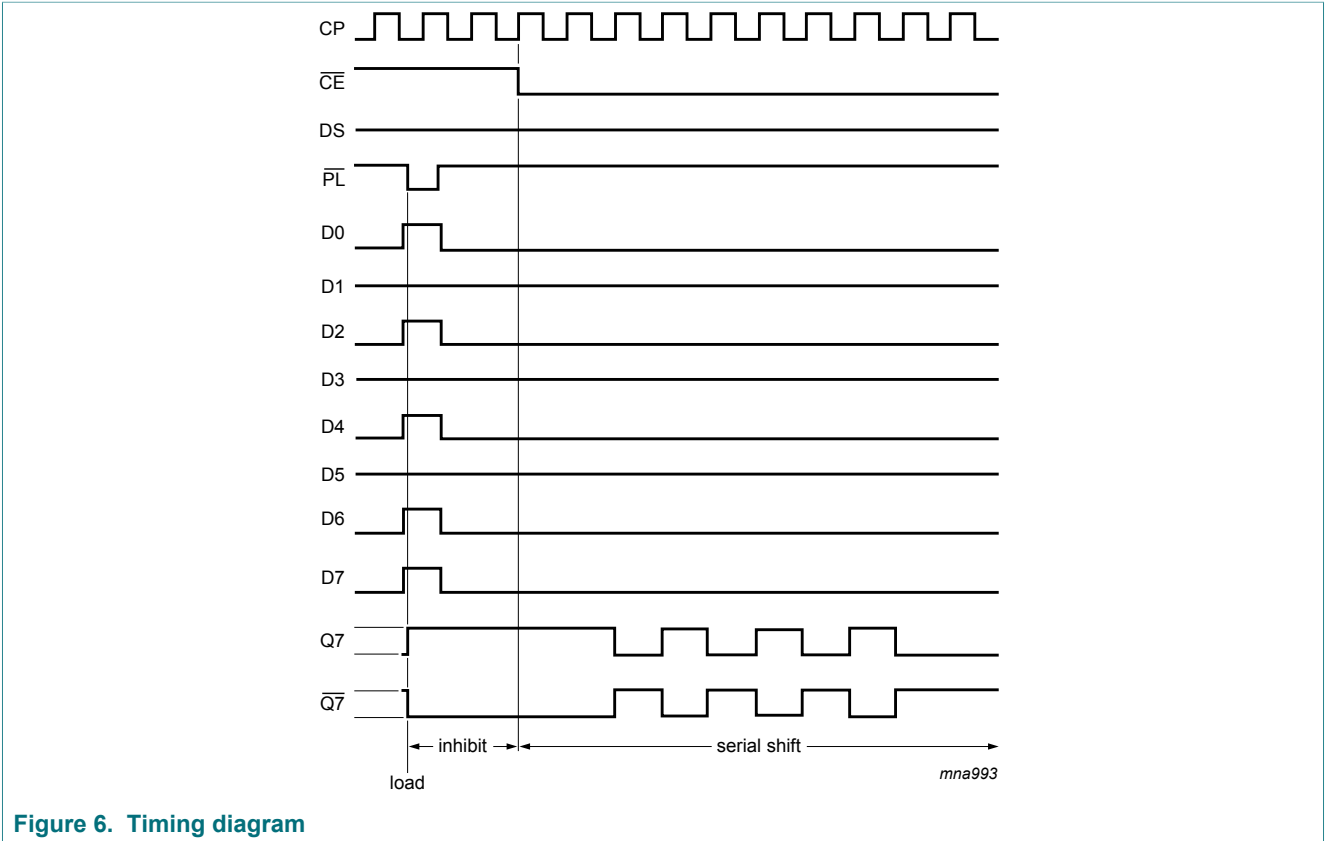


Figure 6. Timing diagram

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|------------------------------------------------------------|------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_O | output current | $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ | - | ± 25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 Packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For (T)SSOP16 Packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN16 Packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9 Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC165 | | | 74HCT165 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | - | +125 | -40 | - | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

10 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|-----------------------------------------------------|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC165 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-------|------|------|------------------|-------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT165 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | Dn and DS inputs | - | 35 | 126 | - | 157.5 | - | 171.5 | μA |
| | | CP \overline{CE} , and \overline{PL} inputs | - | 65 | 234 | - | 292.5 | - | 318.5 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

11 Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);

$C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 12](#)

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------------------------|-------------------|--------------------------------------------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC165 | | | | | | | | | | |
| t_{pd} | propagation delay | CP or \overline{CE} to Q7, $\overline{Q7}$; see Figure 7 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 52 | 165 | - | 205 | - | 250 | ns |
| | | $V_{CC} = 4.5$ V | - | 19 | 33 | - | 41 | - | 50 | ns |
| | | $V_{CC} = 6.0$ V | - | 15 | 28 | - | 35 | - | 43 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 16 | - | - | - | - | - | ns |
| | | \overline{PL} to Q7, $\overline{Q7}$; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 50 | 165 | - | 205 | - | 250 | ns |
| | | $V_{CC} = 4.5$ V | - | 18 | 33 | - | 41 | - | 50 | ns |
| | | $V_{CC} = 6.0$ V | - | 14 | 28 | - | 35 | - | 43 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns |
| | | D7 to Q7, $\overline{Q7}$; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 36 | 120 | - | 150 | - | 180 | ns |
| | | $V_{CC} = 4.5$ V | - | 13 | 24 | - | 30 | - | 36 | ns |
| | | $V_{CC} = 6.0$ V | - | 10 | 20 | - | 26 | - | 31 | ns |
| $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 11 | - | - | - | - | - | ns | | |
| t_t | transition time | Q7, $\overline{Q7}$ output; see Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5$ V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0$ V | - | 6 | 13 | - | 16 | - | 19 | ns |
| t_{W} | pulse width | CP input HIGH or LOW; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0$ V | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | \overline{PL} input LOW; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 5 | - | 20 | - | 24 | - | ns |
| $V_{CC} = 6.0$ V | 14 | 4 | - | 17 | - | 20 | - | ns | | |

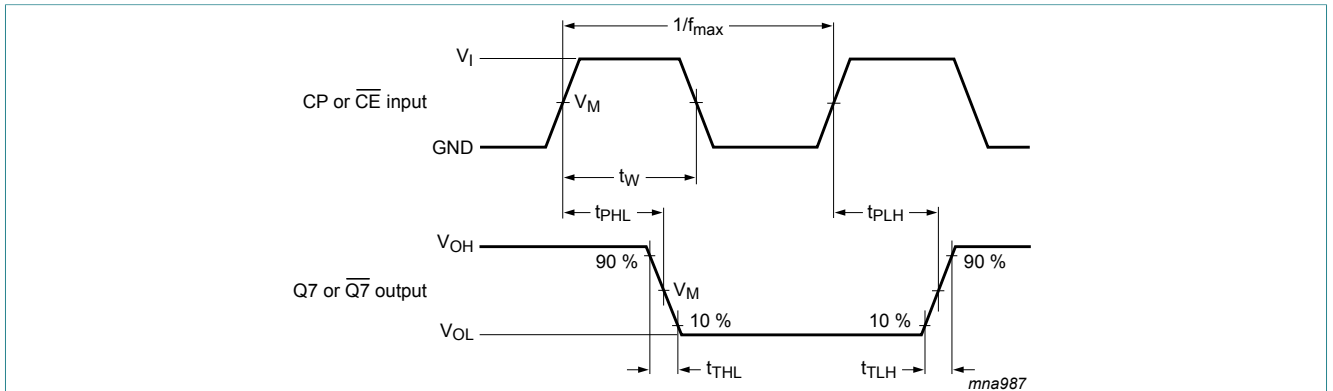
| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{rec} | recovery time | $\overline{\text{PL}}$ to CP, $\overline{\text{CE}}$; see Figure 8 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 100 | 22 | - | 125 | - | 150 | - | ns |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 20 | 8 | - | 25 | - | 30 | - | ns |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 17 | 6 | - | 21 | - | 26 | - | ns |
| t_{su} | set-up time | DS to CP, $\overline{\text{CE}}$; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 80 | 11 | - | 100 | - | 120 | - | ns |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 16 | 4 | - | 20 | - | 24 | - | ns |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 14 | 3 | - | 17 | - | 20 | - | ns |
| | | $\overline{\text{CE}}$ to CP and CP to $\overline{\text{CE}}$; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 14 | 5 | - | 17 | - | 20 | - | ns |
| | | Dn to $\overline{\text{PL}}$; see Figure 11 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 14 | 6 | - | 17 | - | 20 | - | ns |
| t_{h} | hold time | DS to CP, $\overline{\text{CE}}$ and Dn to $\overline{\text{PL}}$; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 5 | 2 | - | 5 | - | 5 | - | ns |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 5 | 2 | - | 5 | - | 5 | - | ns |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 5 | 2 | - | 5 | - | 5 | - | ns |
| | | $\overline{\text{CE}}$ to CP and CP to $\overline{\text{CE}}$; see Figure 10 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 5 | -17 | - | 5 | - | 5 | - | ns |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 5 | -6 | - | 5 | - | 5 | - | ns |
| $V_{\text{CC}} = 6.0 \text{ V}$ | 5 | -5 | - | 5 | - | 5 | - | ns | | |
| f_{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | |
| | | $V_{\text{CC}} = 2.0 \text{ V}$ | 6 | 17 | - | 5 | - | 4 | - | MHz |
| | | $V_{\text{CC}} = 4.5 \text{ V}$ | 30 | 51 | - | 24 | - | 20 | - | MHz |
| | | $V_{\text{CC}} = 6.0 \text{ V}$ | 35 | 61 | - | 28 | - | 24 | - | MHz |
| | | $V_{\text{CC}} = 5.0 \text{ V}$; $C_{\text{L}} = 15 \text{ pF}$ | - | 56 | - | - | - | - | - | MHz |
| C_{PD} | power dissipation capacitance | per package; $V_{\text{I}} = \text{GND to } V_{\text{CC}}$ ^[3] | - | 35 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------|-------------------------------------------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT165 | | | | | | | | | | |
| t _{pd} | propagation delay | \overline{CE} , CP to Q7, $\overline{Q7}$; see Figure 7 ^[1] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 17 | 34 | - | 43 | - | 51 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 14 | - | - | - | - | - | ns |
| | | \overline{PL} to Q7, $\overline{Q7}$; see Figure 8 | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 20 | 40 | - | 50 | - | 60 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 17 | - | - | - | - | - | ns |
| | | D7 to Q7, $\overline{Q7}$; see Figure 9 | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 14 | 28 | - | 35 | - | 42 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 11 | - | - | - | - | ns | |
| t _t | transition time | Q7, $\overline{Q7}$ output; see Figure 7 ^[2] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| t _w | pulse width | CP input; see Figure 7 | | | | | | | | |
| | | V _{CC} = 4.5 V | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | \overline{PL} input; see Figure 8 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 9 | - | 25 | - | 30 | - | ns |
| t _{rec} | recovery time | \overline{PL} to CP, \overline{CE} ; see Figure 8 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 8 | - | 25 | - | 30 | - | ns |
| t _{su} | set-up time | DS to CP, \overline{CE} ; see Figure 10 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 2 | - | 25 | - | 30 | - | ns |
| | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | Dn to \overline{PL} ; see Figure 11 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 10 | - | 25 | - | 30 | - | ns |
| t _h | hold time | DS to CP, \overline{CE} and Dn to \overline{PL} ; see Figure 10 | | | | | | | | |
| | | V _{CC} = 4.5 V | 7 | -1 | - | 9 | - | 11 | - | ns |
| | | \overline{CE} to CP and CP to \overline{CE} ; see Figure 10 | | | | | | | | |
| | | V _{CC} = 4.5 V | 0 | -7 | - | 0 | - | 0 | - | ns |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|-----------------------------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f _{max} | maximum frequency | CP input; see Figure 7 | | | | | | | | |
| | | V _{CC} = 4.5 V | 26 | 44 | - | 21 | - | 17 | - | MHz |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 48 | - | - | - | - | - | MHz |
| C _{PD} | power dissipation capacitance | per package; V _I = GND to V _{CC} - 1.5 V ^[3] | - | 35 | - | - | - | - | - | pF |

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 Σ (C_L × V_{CC}² × f_o) = sum of outputs;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V.

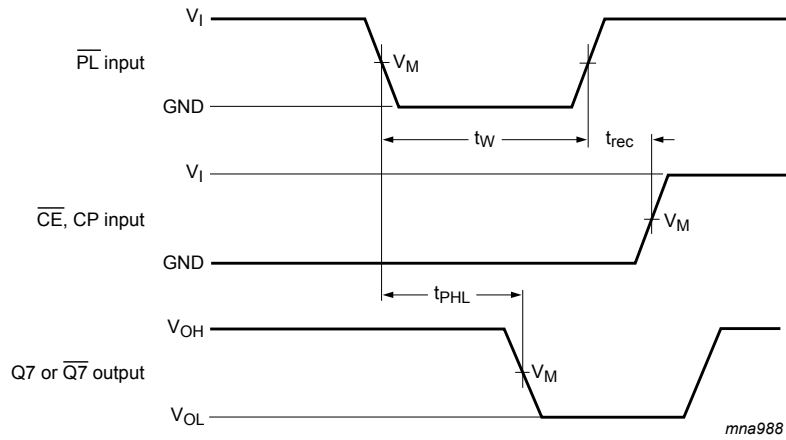
11.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

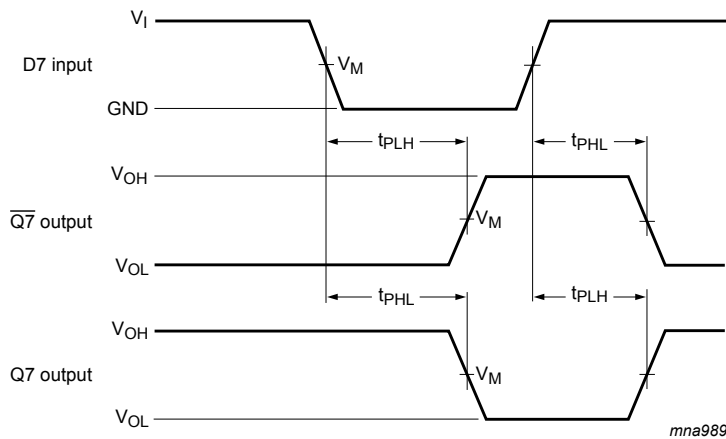
Figure 7. The clock (CP) or clock enable (CE) to output (Q7 or Q7) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

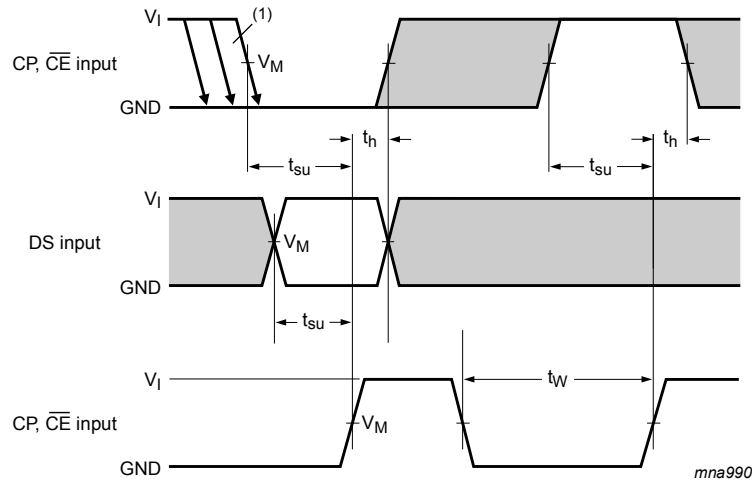
Figure 8. The parallel load (\overline{PL}) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CP) and clock enable (\overline{CE}) recovery time



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 9. The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when \overline{PL} is LOW



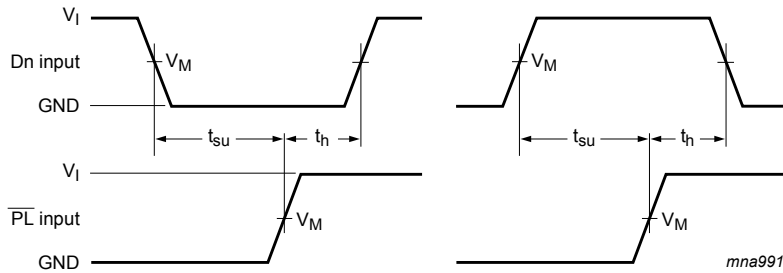
(1) \overline{CE} may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance

Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 10. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable (\overline{CE}) inputs, from the clock enable input (\overline{CE}) to the clock input (CP) and from the clock input (CP) to the clock enable input (\overline{CE})



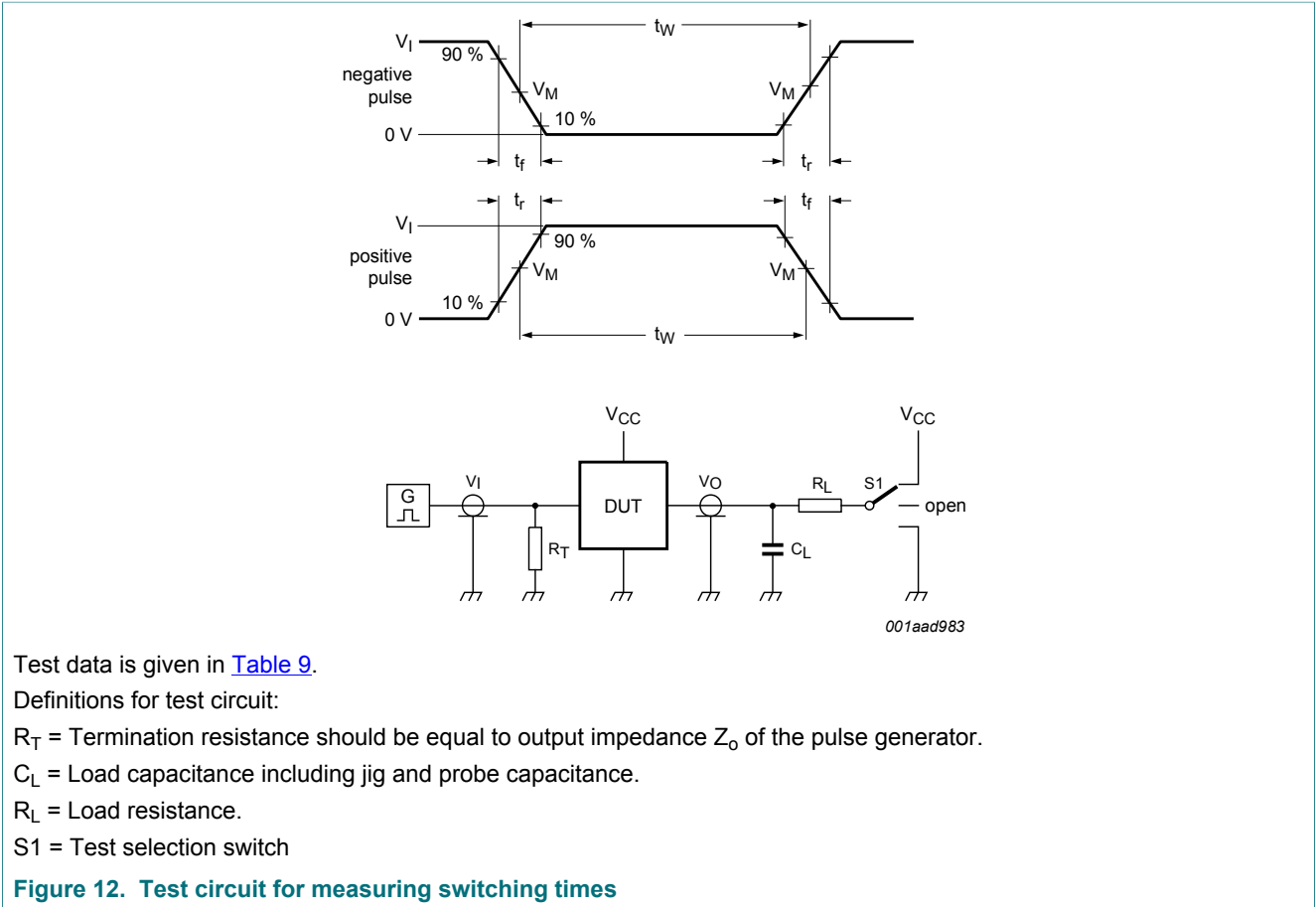
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 11. The set-up and hold times from the data inputs (Dn) to the parallel load input (\overline{PL})

Table 8. Measurement points

| Type | Input | | Output |
|----------|----------|-------------|-------------|
| | V_I | V_M | V_M |
| 74HC165 | V_{CC} | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT165 | 3 V | 1.3 V | 1.3 V |



Test data is given in [Table 9](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch

Figure 12. Test circuit for measuring switching times

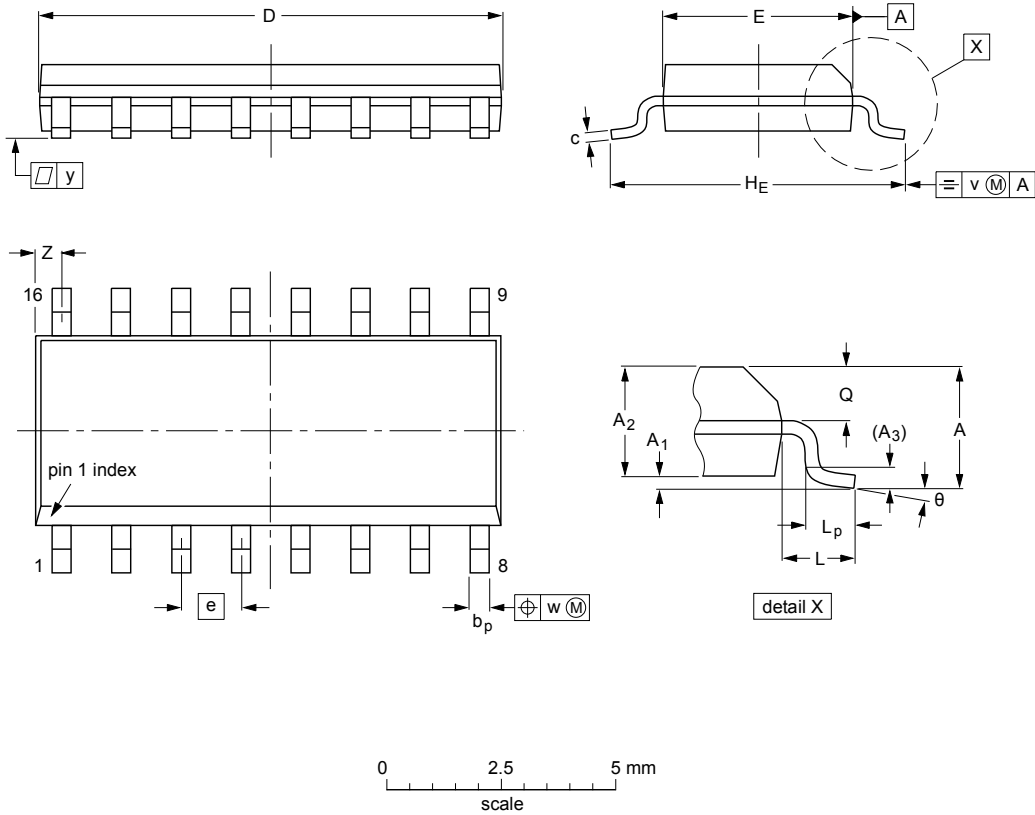
Table 9. Test data

| Type | Input | | Load | | S1 position |
|----------|----------|------------|--------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} |
| 74HC165 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open |
| 74HCT165 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open |

12 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

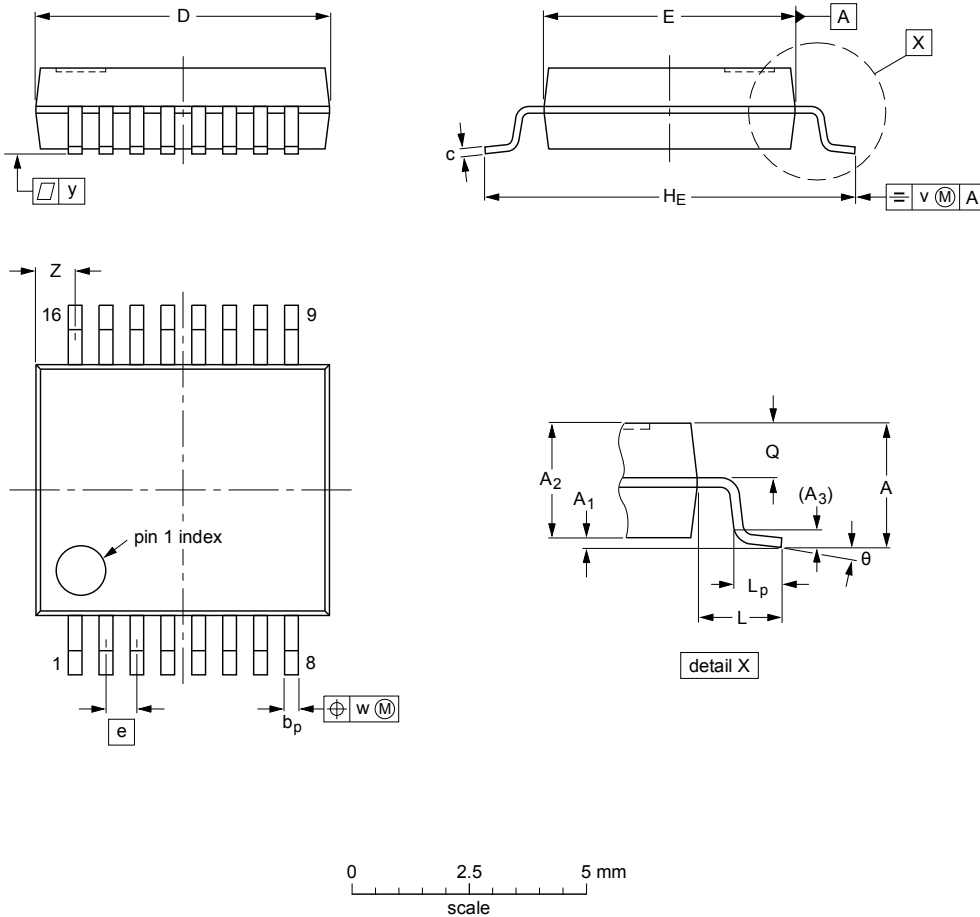
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | |
| SOT109-1 | 076E07 | MS-012 | | | 99-12-27 03-02-19 |

Figure 13. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 6.4 6.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 1.00 0.55 | 8° 0° |

Note

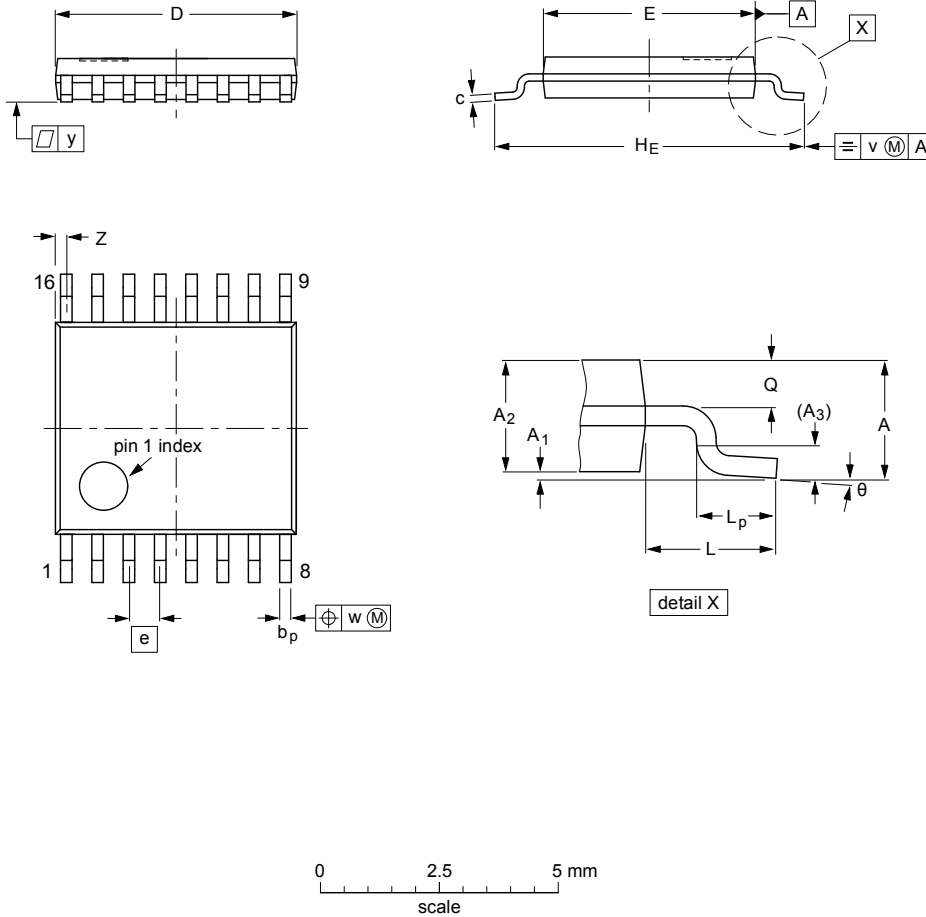
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | 99-12-27 03-02-19 |

Figure 14. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.40 0.06 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|-----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | -99-12-27 03-02-18 |

Figure 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

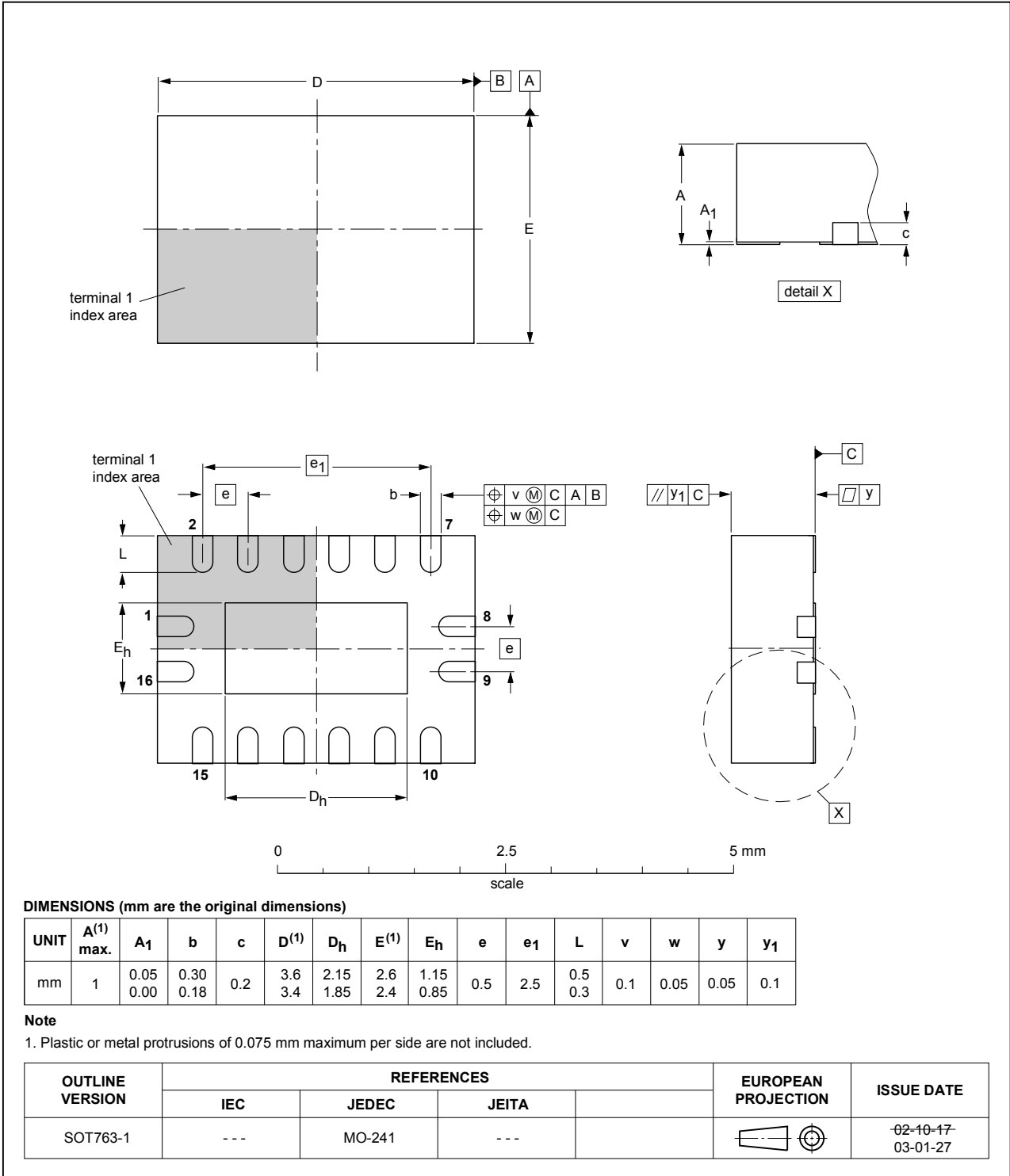


Figure 16. Package outline SOT763-1 (DHVQFN16)

13 Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|-----------------------------------------|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14 Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------|---------------------|
| 74HC_HCT165 v.5 | 20170821 | Product data sheet | - | 74HC_HCT165 v.4 |
| Modifications: | <ul style="list-style-type: none"> Hold time for 74HC165 has been updated. See Paragraph hold time. The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT165 v.4 | 20151228 | Product data sheet | - | 74HC_HCT165 v.3 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC165N and 74HCT165N (SOT38-4) removed. | | | |
| 74HC_HCT165 v.3 | 20080314 | Product data sheet | - | 74HC_HCT165_CNV v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Package SOT763-1 (DHVQFN16) added to Section 4 and Section 12. Family data added, see Section 10 | | | |
| 74HC_HCT165_CNV v.2 | December 1990 | Product specification | - | - |

15 Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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