SN74LV245A 具有三态输出的八路总线收发器

1 特性

- 2V 至 5.5V V_{CC} 运行
- 5V 时 t_{pd} 最大值为 6.5 ns
- V_{OLP}（输出接地反弹）典型值
  小于 0.8V（V_{CC} = 3.3V、T_A = 25°C 时）
- V_{OHV}（输出 V_{OH} 下冲）典型值
  大于 2.3 V（V_{CC} = 3.3V、T_A = 25°C 时）
- 支持所有端口上的混合模式电压运行
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 服务器
- LED 显示屏
- 网络交换机
- 电信基础设施
- 电机驱动器
- I/O 扩展器

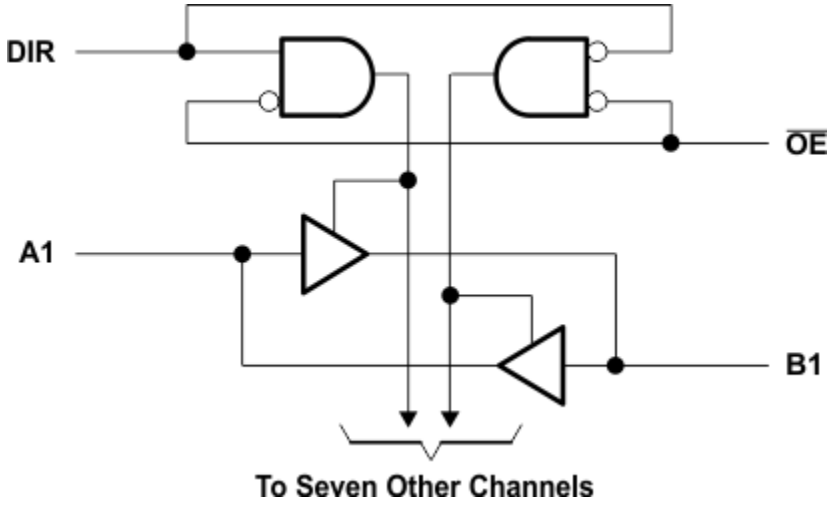
3 说明

这些八路总线收发器旨在于 2V 至 5.5V V_{CC} 下运行。

封装信息(1)

器件型号	封装	封装尺寸（NOM）
SN74LV245A	DB（SSOP，20）	7.20mm × 5.30mm
	DGV（TVSOP，20）	5.00mm × 4.40mm
	PW（TSSOP，20）	6.50mm × 4.40mm
	RGY（VQFN，20）	4.50mm × 3.50mm
	DW（SOIC，20）	12.80mm x 7.50mm
	RKS（VQFN，20）	4.50mm × 2.50mm
	DGS（VSSOP，20）	5.10mm × 3.00mm
	DW（SOIC，20）	12.80mm x 7.50mm
	N（PDIP，20）	24.33mm × 6.35mm
	NS（SO，20）	12.60mm × 5.30mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。



简化版原理图

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Changes from Revision Q (April 2023) to Revision R (July 2023) **Page**

- Updated R θ JA values: DB = 94.6 to 113.1, DW = 77.5 to 96.2, NS = 76.6 to 101.1; Updated DB, DW, and PW packages for R θ JC(top), R θ JB, Ψ JT, Ψ JB, and R θ JC(bot), all values in °C/W 5

Changes from Revision P (December 2022) to Revision Q (April 2023) **Page**

- 添加了 DGS 封装信息 1
- 更新了*封装信息* 表 1

Changes from Revision O (September 2014) to Revision P (December 2022) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 添加了 RKS 封装信息 1

5 Pin Configuration and Functions

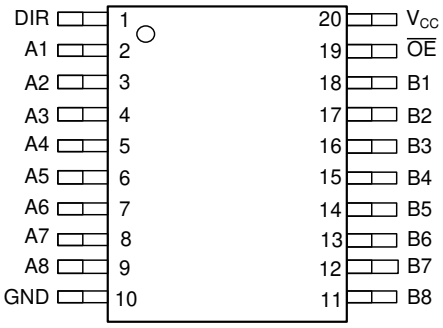


图 5-1. SN74LV245A: DB, DGV, DW, N, NS, PW or DGS, 20-Pin SSOP, TVSOP, SOIC, PDIP, SO, TSSOP, or VSSOP (Top View)

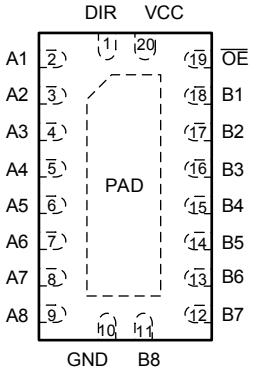


图 5-2. SN74LV245A: RGY or RKS Package, 20-Pin VQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DIR	1	I	Direction Pin
A1	2	I/O	A1 I/O
A2	3	I/O	A2 I/O
A3	4	I/O	A3 I/O
A4	5	I/O	A4 I/O
A5	6	I/O	A5 I/O
A6	7	I/O	A6 I/O
A7	8	I/O	A7 I/O
A8	9	I/O	A8 I/O
GND	10	—	Ground Pin
B8	11	I/O	B8 I/O
B7	12	I/O	B7 I/O
B6	13	I/O	B6 I/O
B5	14	I/O	B5 I/O
B4	15	I/O	B4 I/O
B3	16	I/O	B3 I/O
B2	17	I/O	B2 I/O
B1	18	I/O	B1 I/O
$\overline{OE}$	19	I	Output Enable
V_{CC}	20	—	Power Pin

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	7	V
V_I	Input voltage range	Except I/O ports(2)	– 0.5	7	V
		I/O ports(2) (3)	– 0.5	7	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		– 0.5	7	V
V_O	Output voltage range applied in the high or low state(2) (3)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 20	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		– 65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV245A		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		– 50	μA
		V_{CC} = 2.3 V to 2.7 V		– 2	mA
		V_{CC} = 3 V to 3.6 V		– 8	
		V_{CC} = 4.5 V to 5.5 V		– 16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		– 40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV245A								UNIT
		DB	DGV	DW	NS	PW	RGY	RKS	DGS	
		20 PINS								
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.1	114.8	96.2	101.1	101.5	34.1	67.7	118.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.9	30.1	63.6	67	35.6	38.4	72.4	57.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	67.9	56.3	64.7	66.1	52.5	12.0	40.4	73.1	
ψ_{JT}	Junction-to-top characterization parameter	39.3	0.9	40.5	37.6	2.2	0.8	10.3	5.7	
ψ_{JB}	Junction-to-board characterization parameter	67.5	55.6	64.3	65.8	52.0	12.0	40.4	72.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	7.1	24.1	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–40°C to 85°C SN74LV245A			–40°C to 125°C SN74LV245A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –2 mA	2.3 V	2			2			
		I_{OH} = –8 mA	3 V	2.48			2.48			
		I_{OH} = –16 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4	
		I_{OL} = 8 mA	3 V			0.44			0.44	
		I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	Control inputs	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{OZ}	A or B port	V_O = V_{CC} or GND	5.5 V			±5			±5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}		V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	Control inputs	V_I = V_{CC} or GND	3.3 V		3					pF
			5 V		3					
C_{io}	A or B port	V_O = V_{CC} or GND	3.3 V		5.5					pF
			5 V		5.5					

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		8.3	13	1	15	1	17	ns
t_{en}	$\overline{OE}$	A or B			11.8	19.9	1	22	1	24	
t_{dis}	$\overline{OE}$	A or B			11.8	18.1	1	20	1	22	
t_{pd}	A or B	B or A	C_L = 50 pF		11.2	15.9	1	18	1	21	ns
t_{en}	$\overline{OE}$	A or B			14.1	22.7	1	26	1	28	
t_{dis}	$\overline{OE}$	A or B			17.6	23.1	1	25	1	27	
$t_{sk(o)}$						2		2			

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		5.9	8.4	1	10	1	11	ns
t_{en}	$\overline{OE}$	A or B			8.2	13.2	1	15.5	1	16.5	
t_{dis}	$\overline{OE}$	A or B			9.6	16.5	1	19.5	1	20.5	
t_{pd}	A or B	B or A	C_L = 50 pF		7.9	11.9	1	13.5	1	14.5	ns
t_{en}	$\overline{OE}$	A or B			9.9	16.7	1	19	1	20	
t_{dis}	$\overline{OE}$	A or B			13.9	19.8	1	22	1	23	
$t_{sk(o)}$						1.5		1.5			

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		4.3	5.5	1	6.5	1	7	ns
t_{en}	$\overline{OE}$	A or B			5.7	8.5	1	10	1	10.5	
t_{dis}	$\overline{OE}$	A or B			7.8	12.8	1	14.2	1	14.7	
t_{pd}	A or B	B or A	C_L = 50 pF		5.6	7.5	1	8.5	1	9	ns
t_{en}	$\overline{OE}$	A or B			7	10.6	1	12	1	12.5	
t_{dis}	$\overline{OE}$	A or B			10.9	14.7	1	16	1	16.5	
$t_{sk(o)}$						1		1			

6.9 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74LV245A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

6.10 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	20	pF
					5 V	25	

6.11 Typical Characteristics

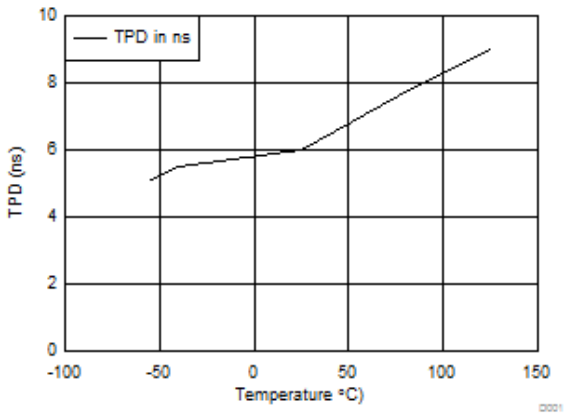


图 6-1. TPD vs Temperature at 3.3 V

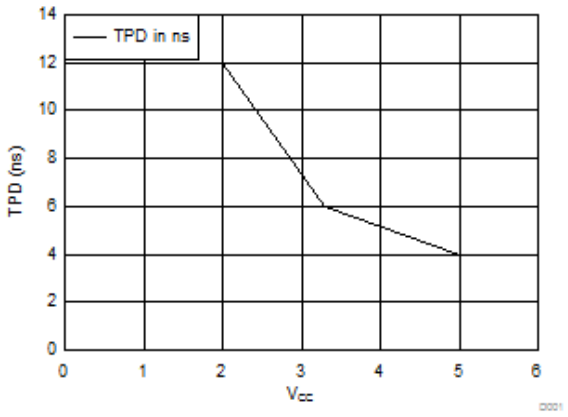
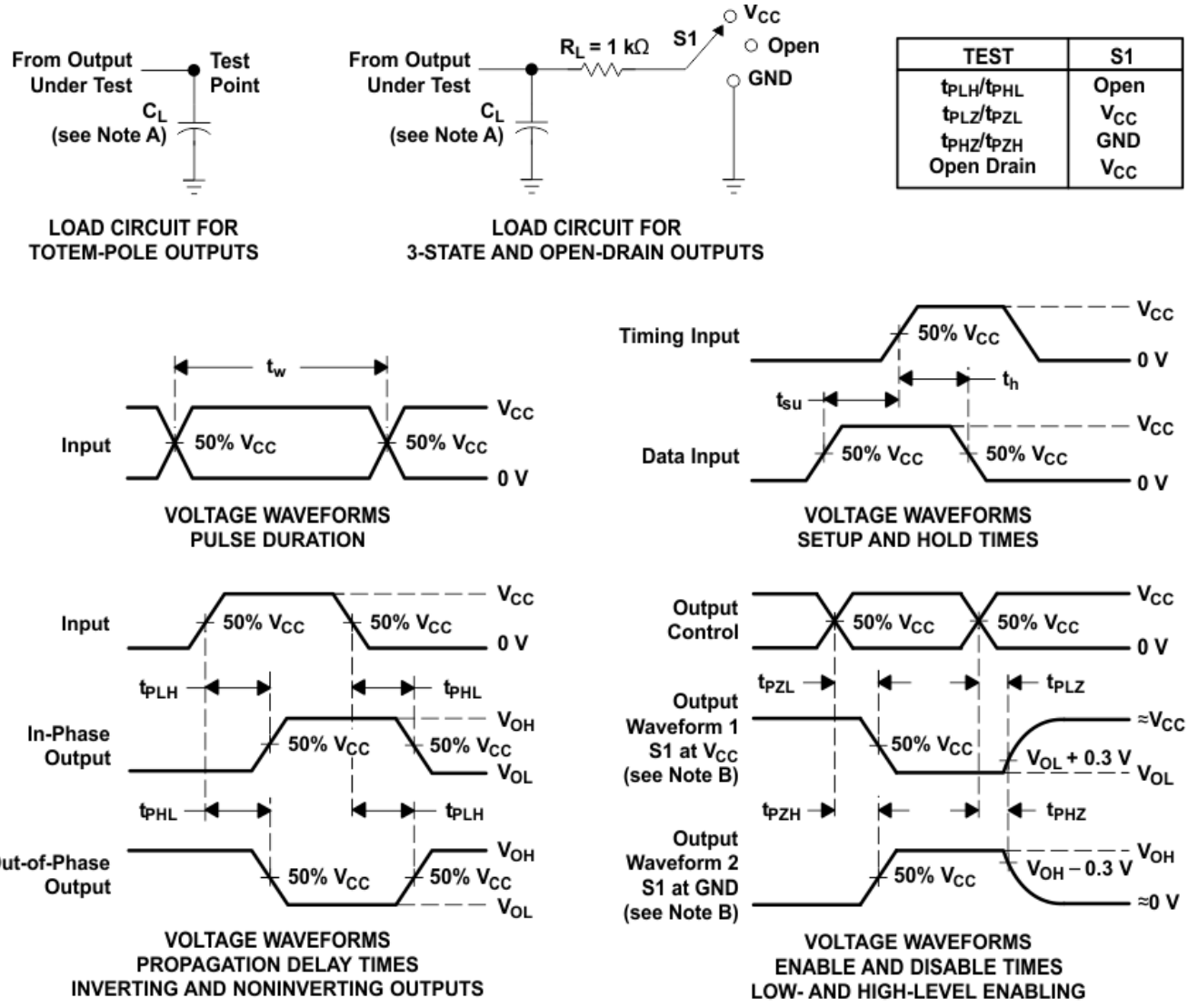


图 6-2. TPD vs V_{CC}

7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

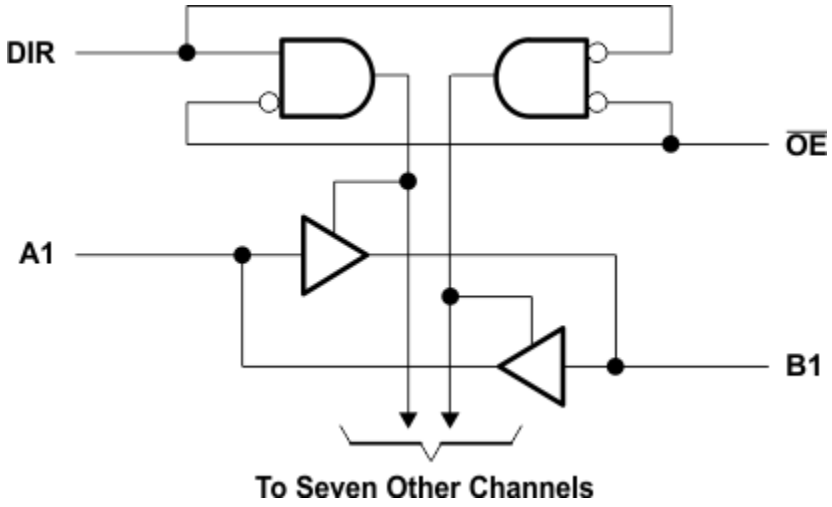


图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- Allows down voltage translation from 5 V to 3.3 V
  - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74LV245A is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making the device ideal for down translation.

9.2 Typical Application

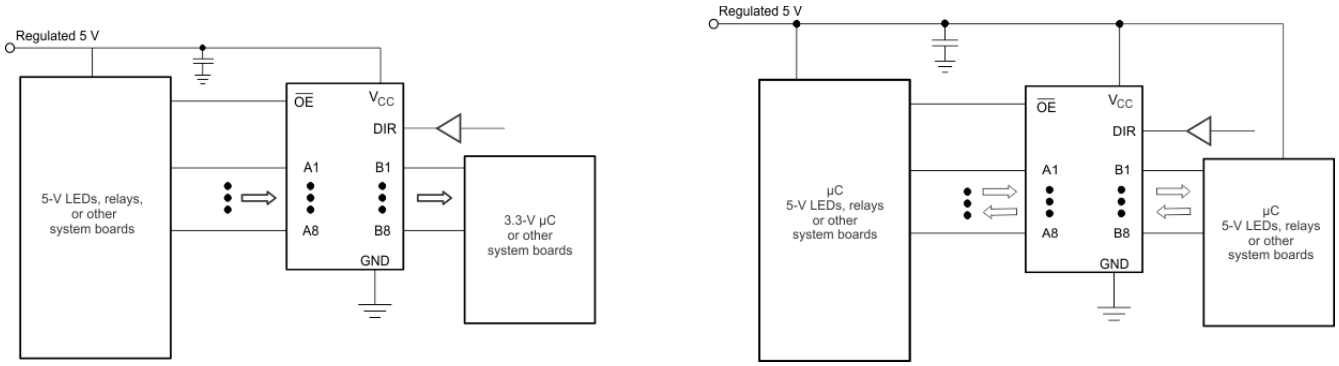


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive will also create faster edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Rise time and fall time specifications, see ($\Delta t/\Delta V$) in *Recommended Operating Conditions* table.
   - Specified high and low levels, see (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend output conditions:
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

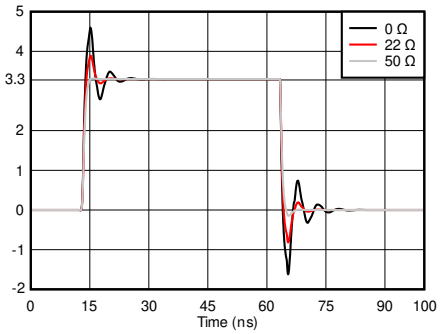


图 9-2. Application Timing Curve

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended and if there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in 图 9-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they cannot float when disabled.

9.4.2 Layout Example

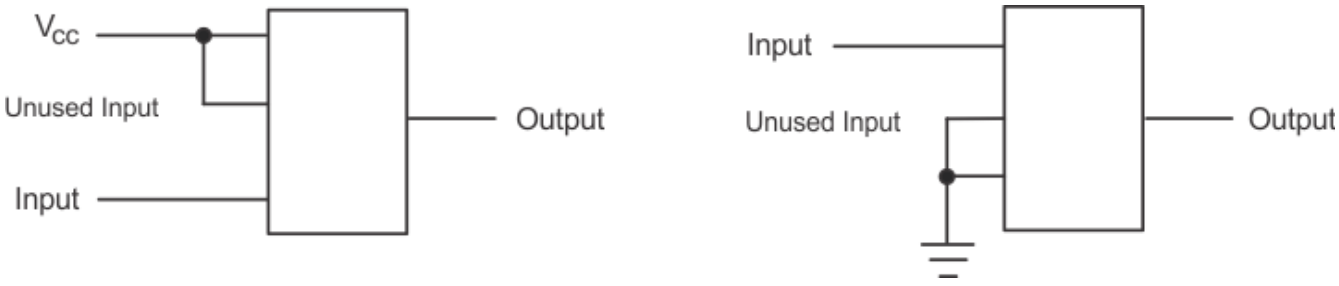


图 9-3. Layout Diagram

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV245ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245ADGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L245A	Samples
SN74LV245ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245ADW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	LV245A	
SN74LV245ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245ANSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV245A	Samples
SN74LV245APW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125	LV245A	
SN74LV245APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245APWRG3	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples
SN74LV245ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV245A	Samples
SN74LV245ARKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要通知和免责声明

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